



User Guide

CCD-CALYPSO • *CompactPCI*®

3U Advanced Pentium® M CPU Board

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2007-02



CCD-CALYPSO

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About this Manual

This manual describes the technical aspects of the CCD-CALYPSO, required for installation and system integration. It is intended for the experienced user only.

Edition History

| Ed. | Contents/Changes | Author | Date |
|-----|--|----------|-------------------|
| 1 | User Manual CCD-CALYPSO, english, initial edition (Text #3946, File: ccd_uge.wpd) | gn | 2005-10-28 |
| 2 | Corrected table of local PCI devices, added section "Hardware Monitor LM87" | gn | 2005-12-02 |
| 3 | Added images CCD-CALYPSO, CCT-RIO | jj | 4 January 2006 |
| 4 | Added chapter "Appendix" containing mechanical drawings | gn | 2006-01-19 |
| 5 | Added image CCD-CALYPSO (top view w/o heatsink) Added image of single slot backplane for SAC/SBC operation | jj | 23 March 2006 |
| 6 | Reworked sections "Reset/Watchdog", "Real-Time Clock", table "GPIO Usage FWH" and table "GPIO Usage ICH6" | gn | 2006-05-05 |
| 7 | Corrected mechanical drawing in chapter "Appendix" (position of PPCIE) Corrected table of expansion interface connector PEXP (pin 40) Updated table "Feature Summary" from latest product info Removed some typos | gn | 2006-07-20 |
| 8 | Added images CCD-CALYPSO w. CCB-BOSSANOVA, C15-DON, CCD-CALYPSO w. C10-CFA Updated table 'Feature Summary' Updated table 'Processors Supported' | jj | 23 August 2006 |
| 9 | Added Performance Score for CCD-2 Added Power Requirements | jj gn | 25 September 2006 |
| 10 | Added +12V connectivity to table of expansion interface connector PEXP (pin 40) and to the table in section "Hardware Monitor LM87". Added photo/section CCE-PUNK, modified illustration 'Front Panel Connectors' | gn jj | 2007-02-13 |
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Related Documents

For information about the CCA-LAMBADA mezzanine companion board refer to the CCA Technical Information Manual, available at http://www.ekf.com/c/ccpu/cca/cca_tie.pdf.

For information about the CCB-BOSSANOVA mezzanine companion board refer to the CCB Technical Information Manual, available at http://www.ekf.com/c/ccpu/ccb/ccb_tie.pdf.

For information about the CCE-PUNK mezzanine companion board refer to the CCE Technical Information Manual, available at http://www.ekf.com/c/ccpu/cce/cce_tie.pdf.

For information regarding the CCT-RIO rear I/O transition module please read the CCT Technical Information Manual, available at http://www.ekf.com/c/ccpu/ccd/cct_tie.pdf.

For ordering information refer to document CCD-CALYPSO Product Information, available at http://www.ekf.com/c/ccpu/ccd/ccd_pie.pdf.

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

- ▶ Intel, Pentium, Celeron, Pentium M, Core Duo: ® Intel
- ▶ *CompactPCI*: ® PICMG
- ▶ Windows 2000, Windows XP: ® Microsoft
- ▶ EKF, ekf system: ® EKF

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

CCD-CALYPSO Features

Feature Summary

| Feature Summary CCD-CALYPSO | |
|-----------------------------|--|
| Form Factor | Single size <i>CompactPCI</i> style Eurocard (160x100mm ²), front panel width 4HP (20.3mm) |
| Processor | <p>Designed for Intel® Pentium® M Micro FC-BGA 479 processors (90nm Dothan), maximum junction temperature 100°C</p> <ul style="list-style-type: none"> ▶ CCD-2: 1.0GHz ULV Celeron® M (Dothan 373), 400MHz FSB, 512KB L2 cache, 5W ▶ CCD-3: 1.4GHz LV Pentium® M (Dothan 738), 400MHz FSB, 2MB L2 cache, 10W ▶ CCD-6: 2.0GHz Pentium® M (Dothan 760), 533MHz FSB, 2MB L2 cache, 27W |
| Chipset | <p>Intel® i915GM chipset (Alviso) consisting of:</p> <ul style="list-style-type: none"> ▶ 82915GM Graphics/Memory Controller Hub (GMCH) with Intel® Graphics Media Accelerator (GMA) 900 ▶ 82801FB I/O Controller Hub (ICH6) ▶ 82802 Compatible Firmware Hub (FWH) |
| Memory | Dual 200-pin SO-DIMM socket, DDR2 533 SDRAM, 2 x 1GB maximum, single or dual channel mode |
| Video | <p>Analog monitor and digital flat-panel display support by DVI-I connector (front panel), up to 2048x1536 pixel 16M colours @75Hz refresh rate (analog), up to 1600 x 1200 pixel 16M colours @60Hz (digital), incorporates PanelLink Digital technology (Silicon Image).</p> <ul style="list-style-type: none"> ▶ Front panel option: D-Sub (female HD15) VGA connector available, replaces DVI-I connector ▶ Rear I/O option: Analog video across J2/P2 CCT-RIO rear I/O transition module) ▶ Dual screen capable 2 x 1600 x 1200 pixel (one display attached to the front panel, the other to the back panel, or both to the front panel by means of a DVI-I splitter cable) |
| USB | <p>All ports over-current protected, data transfer rate of up to 480Mbps, conforming to USB2.0:</p> <ul style="list-style-type: none"> ▶ 2 x USB type A connector (front panel) ▶ 3 x USB ports J2/P2 Rear I/O option (CCT-RIO rear I/O transition module) ▶ 2 x USB ports expansion interface option (CCA-LAMBADA / CCB-BOSSANOVA / CCE-PUNK mezzanine companion board) ▶ USB Flash drive module C15-DON option (USB stick on-board module) |
| Ethernet | Dual 10/100/1000Mbps Gigabit Ethernet controller, accessible via RJ45 jacks from the front panel, or as an option 1 x across J2/P2 with attached CCT-RIO rear I/O transition module |

Feature Summary CCD-CALYPSO

| | | | | | |
|----------------------------|---|--------------------------------|----------------------------------|--------------------------------|----------------------------------|
| Mezzanine I/O | <ul style="list-style-type: none"> On-board LPC/USB/AC97 Super-I/O, USB and audio expansion interface connector ATA/IDE expansion connector High Speed PCI Express expansion connector Suitable mezzanine companion boards available: <ul style="list-style-type: none"> CCA-LAMBADA: Front panel COM, USB, AC'97 audio, PS/2 keyboard/mouse, on board hard disk drive 1.8-inch or 2.5-inch CCB-BOSSANOVA: Front panel up to 2 x COM, up to 2 x USB, PS/2 keyboard/mouse, on board hard disk drive 1.8-inch or 2.5-inch CCE-PUNK: Front panel 2 x COM, 2 x USB, 2 x 1394a FireWire, on board hard disk drive 1.8-inch or 2.5-inch C10-1-CFA CompactFlash adapter module C10-2-CFA 1.8-inch hard disk module C15-DON on-board USB stick module (USB Flash disk) | | | | |
| PATA (IDE) | <ul style="list-style-type: none"> Ultra ATA/100 connector, handover to CCA-LAMBADA / CCB-BOSSANOVA / CCE-PUNK mezzanine expansion board with optional on-board 2.5-inch hard disk drive or external device CompactFlash socket C10-1-CFA supplied for a CFA ATA memory card or Microdrive® Option 1.8-inch on-board hard disk module C10-2-CFA, replaces CompactFlash facility | | | | |
| SATA | Triple-channel Serial ATA I/F available for J2/P2 rear I/O option, suitable rear I/O transition module CCT-RIO (2 x system internal SATA, 1 x eSATA for attachment of external devices) | | | | |
| CompactPCI | ICH6 integrated 32-bit PCI bridge, 133MBps CPCI master | | | | |
| PCI Express | 1-Lane PCIe connector (option) for CCE-PUNK and future mezzanine companion boards | | | | |
| J2/P2 Rear I/O | <ul style="list-style-type: none"> 3 x Serial ATA (SATA), 2 x system internal SATA connectors, 1 x external eSATA connector 1 x GB Ethernet (switched by BIOS between front panel I/O and rear I/O) 3 x USB VGA Analog Video, or GPIO Keyboard, Mouse COM1 (TTL Level) Suitable rear I/O transition module CCT-RIO available | | | | |
| BIOS | <ul style="list-style-type: none"> Phoenix BIOS with EKF enhancements 8Mbit Flash memory Updates available from website ekf.com | | | | |
| Drivers (All Major OS) | <ul style="list-style-type: none"> Intel graphics drivers Intel networking drivers | | | | |
| Typical Power Requirements | | +3.3V +0.17V/-0.1V | | +5V +0.25V/-0.15V | |
| | Board | MaxPower LFM/HFM ¹⁾ | WinXP Idle LFM/HFM ¹⁾ | MaxPower LFM/HFM ¹⁾ | WinXP Idle LFM/HFM ¹⁾ |
| | CCD-2-CALYPSO | 2.7A ²⁾ | 2.2A ²⁾ | 1.2A ²⁾ | 0.5A ²⁾ |
| | CCD-3-CALYPSO | 2.9A/2.9A | 2.2A/2.2A | 1.2A/2.4A | 0.7A/0.9A |
| CCD-6-CALYPSO | 3.0A/3.3A | 2.3A/2.3A | 1.2A/5.2A | 0.7A/1.6A | |

Feature Summary CCD-CALYPSO

| Thermal Conditions Environmental Conditions | <ul style="list-style-type: none"> ▶ Operating temperature: 0°C ... +70°C (CPU dependent) ▶ Storage temperature: -40°C ... +85°C, max. gradient 5°C/min ▶ Humidity 5% ... 95% RH non condensing ▶ Altitude -300m ... +3000m ▶ Shock 15g 0.33ms, 6g 6ms ▶ Vibration 1g 5-2000Hz | | | | | | | | | | | | |
|---|---|---------------|-----------|---------------|---------------|------------------------------------|-----------|---------------|-----------------------------------|-----|---------------|--------------------------------|-----|
| EC Regulations | <ul style="list-style-type: none"> ▶ EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1) ▶ 2002/95/EC (RoHS) | | | | | | | | | | | | |
| MTBF | tbd | | | | | | | | | | | | |
| Performance Rating | <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;">Board</th> <th style="width: 50%;">Processor</th> <th style="width: 25%;">CPU/MEM Score</th> </tr> </thead> <tbody> <tr> <td>CCD-2-CALYPSO</td> <td>1.0GHz ULV Celeron® M (Dothan 373)</td> <td>4735/8642</td> </tr> <tr> <td>CCD-3-CALYPSO</td> <td>1.4GHz LV Pentium® M (Dothan 738)</td> <td>tbd</td> </tr> <tr> <td>CCD-6-CALYPSO</td> <td>2.0GHz Pentium® M (Dothan 760)</td> <td>tbd</td> </tr> </tbody> </table> | Board | Processor | CPU/MEM Score | CCD-2-CALYPSO | 1.0GHz ULV Celeron® M (Dothan 373) | 4735/8642 | CCD-3-CALYPSO | 1.4GHz LV Pentium® M (Dothan 738) | tbd | CCD-6-CALYPSO | 2.0GHz Pentium® M (Dothan 760) | tbd |
| Board | Processor | CPU/MEM Score | | | | | | | | | | | |
| CCD-2-CALYPSO | 1.0GHz ULV Celeron® M (Dothan 373) | 4735/8642 | | | | | | | | | | | |
| CCD-3-CALYPSO | 1.4GHz LV Pentium® M (Dothan 738) | tbd | | | | | | | | | | | |
| CCD-6-CALYPSO | 2.0GHz Pentium® M (Dothan 760) | tbd | | | | | | | | | | | |
| Measured with PCMark2002 under Windows XP, 1GB DDR2 533 | | | | | | | | | | | | | |

- ¹⁾ Intel SpeedStep® Frequency Modes. LFM: Low Frequency Mode, HFM: High Frequency Mode
²⁾ The ULV Celeron® M processor on CCD-2 does not support Intel SpeedStep®, (alwaysHigh Frequency Mode)

Subject to technical changes

Short Description CCD-CALYPSO

Scalable from the ULV Celeron® M processor up to the 2.0GHz Pentium® M, and provided with 2GB dual channel capable DDR2 RAM, the CCD-CALYPSO is a versatile 4HP/3U (single size Eurocard) CompactPCI® CPU board, designed especially for systems which require high performance at low power consumption.

The chipset is based on PCI Express technology and has a powerful dual-screen integrated graphics accelerator. The DVI-I video interface allows for simultaneous attachment of both, advanced (digital) and legacy (analog) flat panel displays and CRT monitors (D-SUB connector optionally).

The CCD-CALYPSO is equipped with two independent PCIe Gigabit Ethernet controllers for high speed communication.

Seven USB 2.0 ports are provided for attachment of peripheral devices. In addition, an on-board CF socket accommodates either a CompactFlash memory card or Microdrive®. As an alternate, an 1.8-inch hard disk module is available as on-board mass-storage device (option).

A local expansion interface connector may be used to directly attach a mezzanine companion board for audio- and legacy support, which can carry in addition a 2.5-inch IDE hard disk drive.

As an option, a rear I/O transition module is available to the CCD-CALYPSO, which e.g. provides the Serial ATA connectors (2 x SATA, 1 x eSATA).

Benefits of the CCD-CALYPSO

- ▶ Pentium® M 2GHz (FSB 533MHz) CompactPCI CPU
- ▶ 2 x 1GB DDR2 Memory (Dual Channel Mode Capable)
- ▶ Dual-Screen Graphics Controller
- ▶ Dual Gigabit Ethernet Controllers
- ▶ Triple SATA I/F
- ▶ Seven USB 2.0 channels
- ▶ On-Board CompactFlash or on-Board 1.8-Inch Hard Disk
- ▶ PCI Express Chipset i915GM Alviso
- ▶ Mezzanine Expansion Board and Rear I/O Transition Module Options
- ▶ RoHS compliant



CCD-CALYPSO w. C10-1 CompactFlash Adapter Module



CCD-CALYPSO w. C10-2 1.8-Inch Hard Disk Module



CompactFlash Adapter Module for CCD-CALYPSO

The CCD-CALYPSO comes with a CompactFlash adapter module, which is suitable to hold a silicon memory CF card or Microdrive hard disk. If the CCD-CALYPSO is accompanied by a mezzanine expansion module such as the CCA-LAMBADA or CCB-BOSSANOVA, the position of the CompactFlash adapter module changes to the mezzanine card.

Optionally an on-board 1.8-inch hard disk module is available. When ordered, it replaces the CompactFlash adapter module (please request for a special solution which allows to use both the CF slot and the 1.8-inch drive simultaneously).



1.8-Inch on-Board Hard Disk Module for CCD-CALYPSO

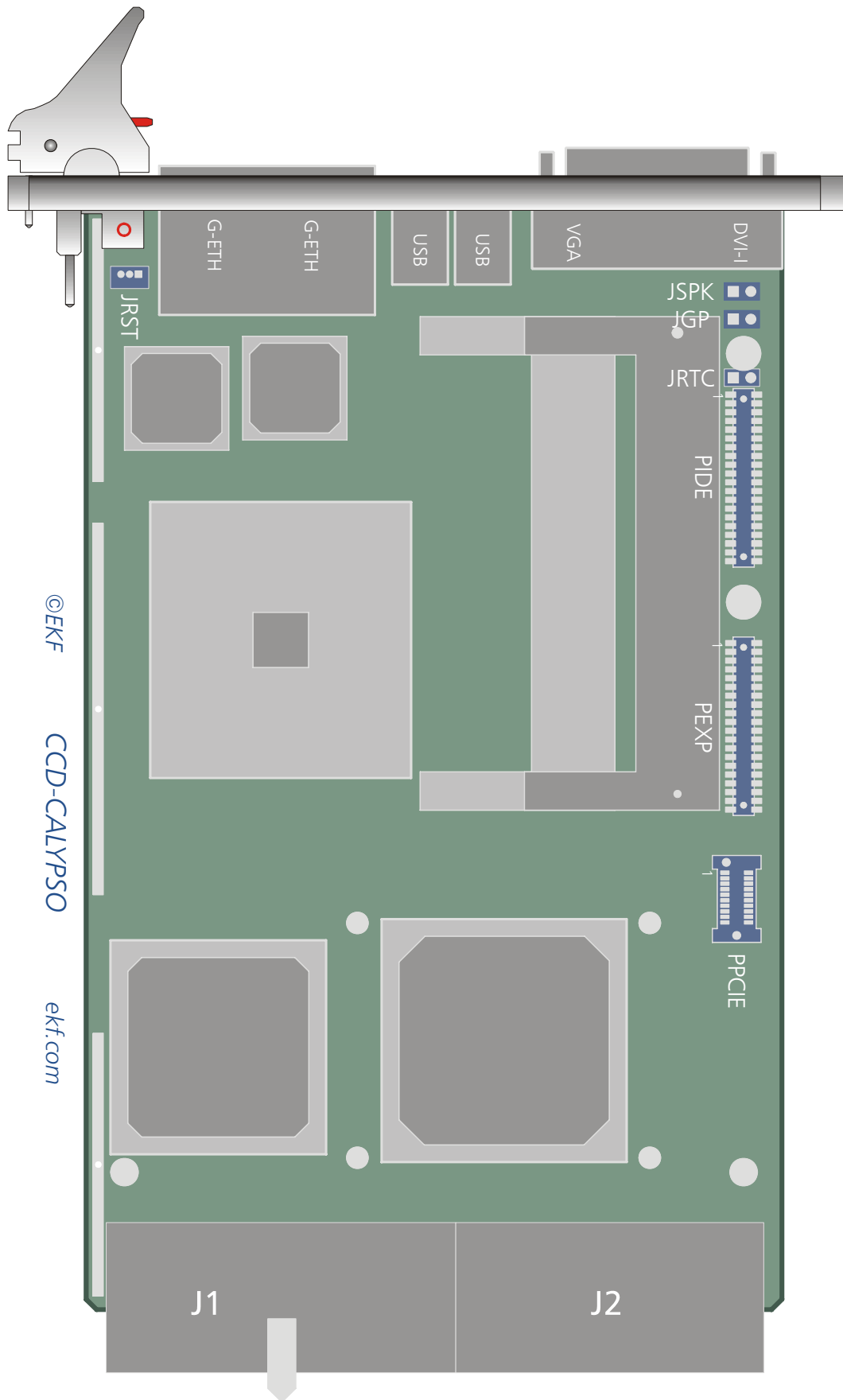


CCD-CALYPSO w. CCB-BOSSANOVA Mezzanine Companion Board & 2.5-Inch HD



USB Flash Drive Option C15

Top View Component Assembly CCD-CALYPSO



Rear I/O Transition Module CCT-RIO

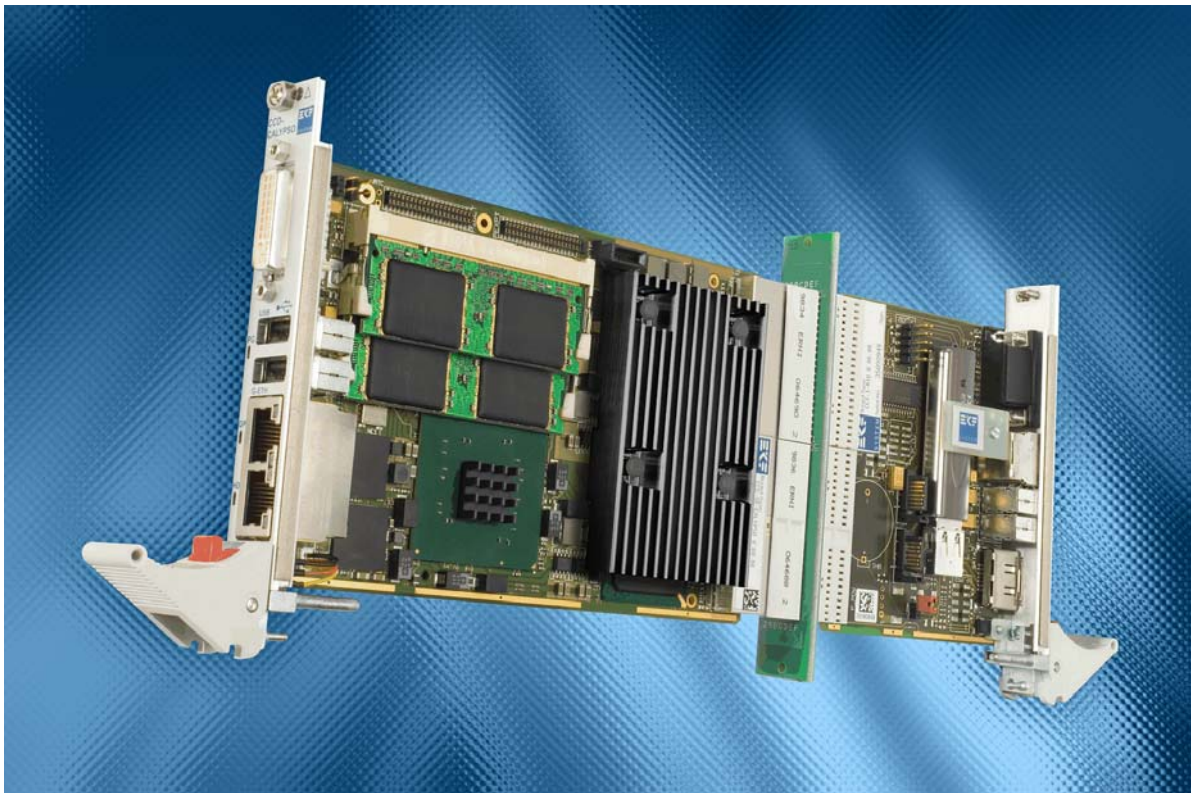
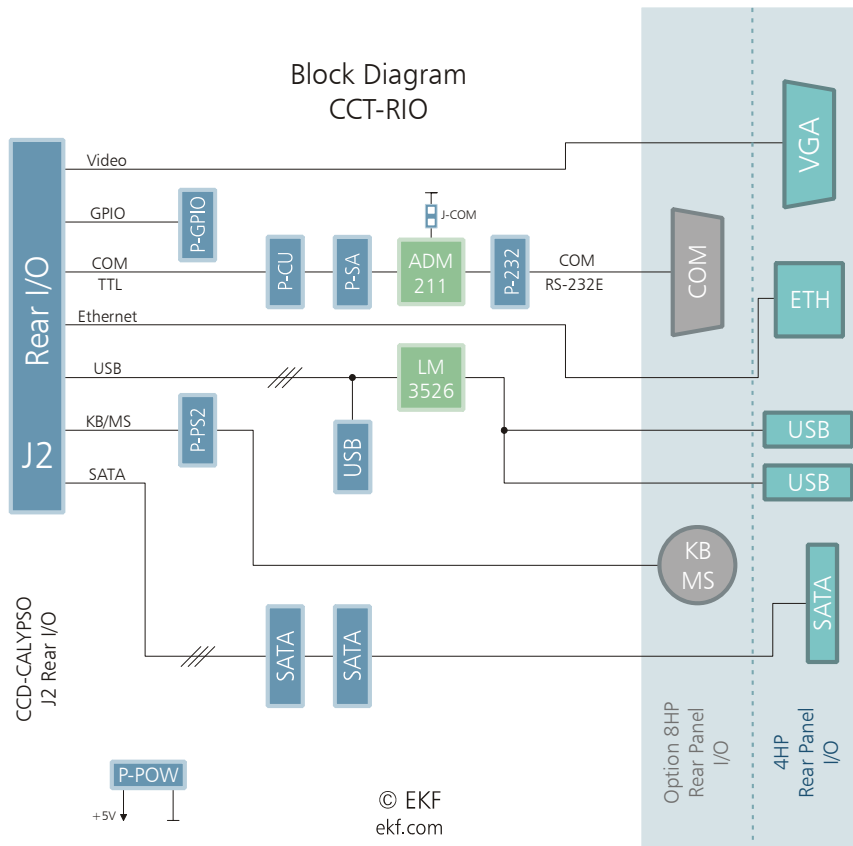
Available as a rear I/O expansion board to the CCD-CALYPSO CPU card, the CCT-RIO is provided with several I/O port connectors, to be used either in addition to the CCD front panel connectors or alternatively. Being mainly a passive rear I/O transition module, groups of signals from the CCD-CALYPSO CPU board are passed across the CompactPCI J2/P2 connector to the CCT-RIO. Some of the data lines are available locally on the CCT board for system internal wiring only, while other connectors such as VGA-Video and Gigabit Ethernet are mounted into the back panel for external use. USB and SATA (eSATA) channels are provided both on-board and externally.

Typically the CCT-RIO is equipped with a 4-HP rear panel (20.3mm width). As a custom specific option, an 8-HP panel is available with additional connectors. Utilization of the CCT-RIO transition module adds a level of I/O functionality that is not available with the CCD-CALYPSO CPU board alone. Further on, swapping the CPU card is simplified by means of rear I/O, which is important for efficient system maintenance (MTTR).

For technical details please refer to the 'CCT-RIO Technical Information Manual', available at www.ekf.com/c/ccpu/ccd/cct_tie.pdf.



CCT-RIO (Shown with on-Board USB Stick)



CCD-CALYPSO with CCT-RIO

CCE-PUNK Mezzanine Module

Available as a mezzanine companion board to the CCD-CALYPSO CPU card, the CCE-PUNK is provided with high-speed communication channels such as FireWire™ and USB, and common legacy I/O ports as well. Interconnection between the CCE-PUNK I/O module and the CPU carrier board is achieved by several expansion connectors, which comprise the PCIe (PCI Express), LPC (Low Pin Count) and ATA/IDE interfaces.

As an option, the CCE-PUNK is available with a rugged on-board 2.5-inch hard disk drive (1.8-inch as a mezzanine module).

The CCE-PUNK will be attached on top of the CPU board, and shares its front panel typically with the host CPU carrier board (8HP front panel width in total).



CCD-CALYPSO CPU Board with CCE-PUNK Mezzanine Companion Module

Strapping Headers

| | |
|--------|---|
| ISPCON | PLD Programming Connector, not stuffed |
| JGP | Jumper to Reset BIOS CMOS RAM Values |
| JRST | Jumper to Reset Board |
| JRTC | Jumper to Reset RTC Core of ICH6, not stuffed |
| JSPK | Speaker Connector |

Connectors & Sockets

| | |
|--------------------|--|
| J1/J2 | <i>CompactPCI</i> Bus 32-bit, 33MHz, PXI, Rear I/O |
| PEXPT PEXPB | Expansion Interface Connector (LPC Interface (2 nd Super-I/O, 2 nd FWH), USB Interfaces, AC'97 Interface, GPIOs), available either from top (T) or bottom (B) of the board |
| PIDET PIDEB | Ultra ATA/100 IDE Port (Interface to CompactFlash ATA Socket on C10-CFA), available either from top (T) or bottom (B) of the board |
| PITP | CPU Debug Port |
| PPCIE | PCI Express Expansion Interface Connector |
| SODIMM1 SODIMM2 | 200-pin DDR2 Memory Module SDRAM PC2-3200/4200 (DDR400/533) Sockets |

Front Panel Elements

| | |
|------------------|---|
| Ethernet (G-ETH) | Dual 1000Base-TX/100Base-TX/10Base-T, RJ-45 Receptacles with integrated indicator LEDs |
| Graphics (DVI-I) | DVI-I Integrated (digital & analog) Receptacle, suitable for DVI digital flat panel displays and/or analog monitors |
| USB1/2 | Universal Serial Bus 2.0 self powered root hub, type A receptacle |
| GP | General Purpose LED |
| HD | LED indicating any activity on IDE or SATA ports |
| PG | LED indicating Power Good/Board Healthy |

Microprocessor

The CCD-CALYPSO is designed for use with Pentium® M and Celeron® M processors manufactured in 0.09µ technology (Dothan). These includes also the Ultra Low-Voltage (ULV) Celeron® M and the Low-Voltage (LV) Pentium® M processors as listed below. The processors are housed in a Micro FC-BGA package for direct soldering to the PCB, i.e. the CPU chip cannot be removed or changed by the user.

The processors supported by the CCD-CALYPSO are running at FSB clock speeds of 400MHz and 533MHz. The internal Pentium M processor speed is achieved by multiplying the host bus frequency by a variable value. The multiplier is chosen by currently required performance and the actual core temperature. This technology is called Enhanced Intel SpeedStep®.

Power is applied across the *CompactPCI* connectors J1 (3.3V, 5V). The processor core voltage is generated by a switched voltage regulator, sourced from the 5V plane. The processor signals its required core voltage by 6 dedicated pins according to Intels IMVP-IV voltage regulator specification.

| 0.09µ (Dothan) Processors Supported | | | | | | | | |
|-------------------------------------|---------------------|----------------|---------------|---------|---------------|----------------|------------|----------------|
| Processor | Speed min/max [GHz] | Host Bus [MHz] | L2 Cache [MB] | TDP [W] | Die Temp [°C] | CPU ID | Stepping | sSpec |
| ULV Celeron M 373 ^{1) 2)} | 1.0/1.0 | 400 | 0.5 | 5 | 0-100 | 06D8h | C-0 | SL8LW |
| LV Pentium M 738 ²⁾ | 0.6/1.4 | 400 | 2 | 10 | 0-100 | 06D6h 06D8h | B-0 C-0 | SL7P9 SL89N |
| Pentium M 745 ²⁾ | 0.6/1.8 | 400 | 2 | 21 | 0-100 | 06D6h 06D8h | B-0 C-0 | SL7Q6 SL8U8 |
| Pentium M 760 ²⁾ | 0.8/2.0 | 533 | 2 | 27 | 0-100 | 06D8h | C-0 | SL869 |

- ¹⁾ This processor does not support SpeedStep® technology, since it runs at a fixed core speed.
- ²⁾ Following the Intel Embedded Roadmap, this processor is recommended for long time availability.

Thermal Considerations

In order to avoid malfunctioning of the CCD-CALYPSO, take care of appropriate cooling of the processor and system, e.g. by a cooling fan suitable to the maximum power consumption of the CPU chip actually in use. Please note, that the processors temperature is steadily measured by a special controller (LM87), attached to the onboard SMBus® (System Management Bus). A second temperature sensor internal to the LM87 allows for acquisition of the boards surface temperature. Beside this the LM87 also monitors most of the supply voltages. A suitable software to display both, the temperatures as well as the supply voltages, is MBM (Motherboard Monitor), which can be downloaded from the web. After installation, both temperatures and voltages can be observed permanently from the Windows taskbar.

The CCD-CALYPSO is equipped with a passive heatsink. Its height takes into account the 4HP limitation in mounting space of a CPCI board. In addition, a forced vertical airflow through the system enclosure (e.g. bottom mount fan unit) is strongly recommended ($> 15\text{m}^3/\text{h}$ or 200LFM around the CPU slot). As an exception, the CCD-2-CALYPSO (ULV Celeron M 1GHz) can be operated with natural convection only. Be sure to thoroughly discuss your actual cooling needs with EKF. Generally, the faster the CPU speed the higher its power consumption. For higher ambient temperatures, consider increasing the forced airflow to 400 or 600LFM.

The table showing the supported processors above give also the maximum power consumption (TDP = Thermal Design Power) of a particular processor. Fortunately, the power consumption is by far lower when executing typical Windows or Linux tasks. The heat dissipation increases when e.g. rendering software like the Acrobat Distiller is executed.

The Pentium M processors support Intel's Enhanced SpeedStep® technology. This enables dynamic switching between multiple core voltages and frequencies depending on core temperature and currently required performance. The processors are able to reduce their core speed and core voltage in up to 8 steps down to 600MHz. This leads to an obvious reduction of power consumption (max. 7.5W @600MHz) resulting in less heating. This mode of lowering the processor core temperature is called TM2 (TM=Thermal Monitor). Note, that TM2 is not supported by Celeron M processors.

Another way to reduce power consumption is to modulate the processor clock. This mode (TM1) is supported also by the Celeron M processors and is achieved by actuating the 'Stop Clock' input of the CPU. A throttling of 50% e.g. means a duty cycle of 50% on the stop clock input. However, while saving considerable power consumption, the data throughput of the processor is also reduced. The processor works at full speed until the core temperature reaches a critical value. Then the processor is throttled by 50%. As soon as the high temperature situation disappears the throttling will be disabled and the processors runs at full speed again.

A similar feature is embedded within the Graphics and Memory Controller (GMCH) i915GM. An on-die temperature sensor is used to protect the GMCH from exceeding its maximum junction temperature ($T_{j,max} = 105^\circ\text{C}$) by reducing the memory bandwidth.

These features are controllable by BIOS menu entries. By default the BIOS of the CCD-CALYPSO enables mode TM2 which is the most efficient.

Main Memory

The CCD-CALYPSO is equipped with two sockets for installing 200-pin SO-DIMM modules (module height = 1.25 inch). Supported are unbuffered DDR2 SO-DIMMs ($V_{CC}=1.8V$) without ECC featuring on-die termination (ODT), according the PC2-3200 or PC2-4200 specification. Minimum memory size is 128MB; maximum memory size is 2GB. Due to the video requirements of the i915GM chipset, a minimum of 2x256MB of memory is recommended for the operating systems Windows NT 4.0, Windows 2000 or Windows XP (some of the system memory is dedicated to the graphics controller). The contents of the SPD EEPROM on the SO-DIMMs is used by the BIOS at POST (Power-on Self Test) to program the memory controller within the chipset.

The i915GM chipset supports symmetric and asymmetric memory organization. The maximum memory performance can be obtained by using the symmetric mode. To achieve this mode two SO-DIMMs of equal capacity must be installed in the memory sockets. In asymmetric mode different memory modules may be used with the drawback of less bandwidth. A special case of asymmetric mode is to populate only one memory module (i.e. one socket may be left empty).

LAN Subsystem

The Ethernet LAN subsystem is composed of two Intel 82573 Gigabit Ethernet controllers that provide also legacy 10Base-T and 100Base-TX connectivity. The Ethernet ports are fed to two RJ45 jacks located in the front panel. Each port includes the following features:

- One PCI Express lane per Ethernet controller (250MB/s)
- 1000Base-Tx (Gigabit Ethernet), 100Base-TX (Fast Ethernet) and 10Base-T (Classic Ethernet) capability
- Half- or full-duplex operation
- IEEE 802.3 \square Auto-Negotiation for the fastest available connection
- Jumperless configuration (complete software-configurable)
- Two bicoloured LEDs integrated into the dedicated RJ-45 connector to signal the LAN link, the LAN connection speed and activity status.

Each NIC (Networking Interface Controller) is connected by a single PCI Express lane to the chipset (ICH6). Their MAC addresses (unique hardware number) are stored in dedicated EEPROMs. The Intel Ethernet software and drivers for the 82573 is available from Intel's World Wide Web site for download.

Serial ATA Interface (SATA)

The CCD-CALYPSO provides three serial ATA (SATA) ports each capable of transferring 150MB/s. Integrated within the ICH6 the SATA controller features different modes to support also legacy operating systems. The SATA channels are routed to the CompactPCI J2 connector, thus they are accessible via the rear I/O transition module CCT-RIO.

A LED named HD located in the front panel, signals disk activity status of the SATA and IDE devices.

Available for download from Intel's web site are drivers for popular operating systems, e.g. Windows® 2000, Windows® XP and Linux.

Enhanced IDE Interface

The EIDE interface handles the exchange of information between the processor and peripheral devices like hard disks, ATA CompactFlash cards and CD-ROM drives. The interface supports:

- Up to two ATA devices
- PIO Mode 3/4, Ultra ATA/33, Ultra ATA/66, Ultra ATA/100

The IDE interface is routed to the on-board connectors PIDE_T and PIDE_B (T:top side, B:bottom side of the board). PIDE is used to interface to the CompactFlash Card adapter C10-CFA or to the expansion board CCA-LAMBADA. Use the C10-CFA adapter to attach a CompactFlash ATA style silicon disk, whenever a hard disk is not suitable for your system, or as an additional mass storage device. The CCA-LAMBADA expansion board is capable to carry an on-board 1.8" or 2.5" hard disk drive. When using the 1.8" option the concurrent operation of a CompactFlash device is possible.

A LED named HD located in the front panel, signals disk activity status of the IDE and SATA devices.

The IDE controller is integrated into the ICH6. Ultra ATA IDE drivers can be downloaded from the Intel web site.

Graphics Subsystem

The graphics subsystem is part of the Intel i915GM Graphics/Memory Controller Hub (GMCH). The CCD-CALYPSO is provided with a DVI-I graphics connector. This is both a digital and analog interface. Recent digital input flat-panel displays are widely available with this connector style. For classic monitors, adapters or adapter cables can be used for converting from DVI-I to the 15-pin HD D-SUB connector.

A special display transmitter chip is used to convert Intel's proprietary, PCI express based SDVO interface to the differential DVI signals. The SiI1362 (Silicon Image) transmitter uses PanelLink® Digital technology to support displays ranging from VGA to UXGA resolutions (25 - 165Mpps) in a single link interface.

The GMCH supports several video resolutions and refresh rates. A partial list is contained in the table below. Please note, that flat-panel displays should be operated with their maximum resolution at 60Hz refresh rate.

Partial List of i915GM GMCH Video Modes (analog / digital)

| Resolution | 60Hz | 70Hz | 72Hz | 75Hz | 85Hz |
|------------|---------------------|-------|-------|-------|-------|
| 640x480 | ✓ / ✓ | ✓ / ✓ | ✓ / ✓ | ✓ / ✓ | ✓ / ✓ |
| 800x600 | ✓ / ✓ | ✓ / ✓ | ✓ / ✓ | ✓ / ✓ | ✓ / ✓ |
| 1024x768 | ✓ / ✓ ¹⁾ | ✓ / ✓ | ✓ / ✓ | ✓ / ✓ | ✓ / ✓ |
| 1280x1024 | ✓ / ✓ ¹⁾ | ✓ / ✓ | ✓ / ✓ | ✓ / ✓ | ✓ / ✓ |
| 1600x1200 | ✓ / ✓ ¹⁾ | ✓ / - | ✓ / - | ✓ / - | ✓ / - |
| 2048x1536 | ✓ / - | ✓ / - | ✓ / - | ✓ / - | - / - |

¹⁾ This video mode is suitable for popular flat-panel displays.

As an option, the CCD-CALYPSO can be equipped with an ordinary HD D-Sub 15-lead connector (VGA style). This connector is suitable for analog signals only, so the PanelLink transmitter is not stuffed with this option. Nevertheless also flat-panel displays can be attached to the D-Sub connector but with minor reduced image quality.

Independent from the video connector actually in use, DVI or VGA, the VESA DDC 2B standard is supported. This is a two-wire serial bus (clock, data), which is controlled by the GMCH and allows to read out important parameters, e.g. the maximum allowable resolution, from the attached monitor. In addition, DDC Power (+5V) is delivered to either connector. A resettable fuse is stuffed to protect the board from an external short-circuit condition (0.75A).

Graphics drivers for the i915GM can be downloaded from the Intel web site.

Real-Time Clock

The CCD-CALYPSO has a time-of-day clock and 100-year calendar, integrated into the ICH6. A battery on the board keeps the clock current when the computer is turned off. The CCD uses a BR2032 lithium battery soldered in the board, giving an autonomy of more than 3 years. Under normal conditions, replacement should be superfluous during lifetime of the board.

Universal Serial Bus (USB)

The CCD-CALYPSO is provided with seven USB ports, all of them are USB 2.0 capable. Two USB interfaces are routed to front panel connectors, two ports are feed to the expansion board interface connectors PEXP, and three ports are optionally available for rear I/O across the J2/P2 *CompactPCI* connector.

The front panel USB connectors can source up to 0.5A/5V each, over-current protected by two electronic switches. Protection for the USB ports on the expansion interface and on the rear I/O connector is located on the CCA-LAMBADA and the CCT-RIO respective. The USB controllers are integrated into the ICH6.

LPC Super-I/O Interface

In a modern system, legacy ports as PS/2 keyboard/mouse, COM1/2 and LPT have been replaced by USB and Ethernet connectivity. The 1.4MB floppy disk drive has been swapped against LS-120 or CD-RW drives, attached to a SATA connector, or USB memory sticks. Hence, the CCD-CALYPSO is virtually provided with all necessary I/O ports. However, for compatibility purposes the CCD is additionally equipped with a simple Super-I/O chip, for optional rear I/O of PS/2 keyboard/mouse and COM1 (TTL level only) across the J2/P2 CPCI connector. The Super-I/O controller resides on the local LPC bus (LPC = Low Pin Count interface standard), which is a serialized ISA bus replacement.

As an alternative, EKF offers the CCA-LAMBADA, an expansion module to the CCD-CALYPSO, featuring all classic Super-I/O functionality. The CCA-LAMBADA is a 3U Eurocard with a 4HP (single) width front panel. Access to the connectors PS/2 (mouse, keyboard), COM, USB and audio in/out is given directly from the front panel. The CCA-LAMBADA connects to the CCD-CALYPSO across the connector PEXPT or PEXPB. The CCA-LAMBADA can be attached either to the top or to the bottom of the CCD-CALYPSO.

Reset/Watchdog

The CCD-CALYPSO is provided with two supervisor circuits to monitor the supply voltages 1.8V, 3.3V, 5V, and to generate a clean power-on reset signal.

Due to lack of space within the front panel the CCD-CALYPSO does not offer a classical push button to force a manual board reset. Nevertheless it is possible to reset the board manually. The handle within the front panel contains a micro switch that is used to generate a board reset signal. By pressing the handle's red push button a short reset pulse is triggered. To generate another reset the handle must be closed and unlocked again. The manual reset could be passivated on customers request.

An alternative (and recommended) way to generate a system reset is to activate the signal PRST# located on CompactPCI connector J2 pin C17. Pulling this signal to GND will have the same effect as to push the handle's red push button.

The healthy state of the CCD-CALYPSO is signalled by the LED PG (Power Good) located in the front panel. As soon as this LED begins to shine all power voltages are within their specifications and the reset signal has been deasserted.

An important reliability feature is the watchdog function, which is programmable by software. The behaviour of the watchdog is defined within the PLD, which activates/deactivates the watchdog and controls its time-out period. The time-out delay is adjustable in the steps 2, 10, 50 and 255 seconds. After alerting the WD and programming the time-out value, the related software (e.g. application program) must trigger the watchdog periodically. All watchdog related functions are made available by calling service requests within the BIOS.

The watchdog is in a passive state after a system reset. There is no need to trigger it at boot time. The watchdog is activated on the first trigger request. If the duration between two trigger requests exceeds the programmed period, the watchdog times out and a system reset will be generated. The watchdog remains in the active state until the next system reset. There is no way to disable it once it had been put on alert, whereas it is possible to reprogram its time-out value at any time.

Firmware Hub (Flash BIOS)

The BIOS is stored in an 82802 8Mbit Firmware Hub (there are second sources in use with deviant part numbers). The firmware hub contains a nonvolatile memory core based on flash technology, allowing the BIOS to be upgraded.

The FWH can be reprogrammed (if suitable) by a DOS based tool. This program and the latest CCD-CALYPSO BIOS are available from the EKF website. Read carefully the enclosed instructions. If the programming procedure fails e.g. caused by a power interruption, the CCD-CALYPSO may no more be operable. In this case you would have to send in the board, because the BIOS is directly soldered to the PCB and cannot be changed by the user.

PG (Power Good) LED

The CCD-CALYPSO offers a software programmable LED labelled PG located within the front panel. After system reset, this LED defaults to signal the board healthy respective power good state. This LED changes its function by calling an appropriate BIOS request and is then controlled by software only. The PG LED remains in the programmable state until the next system reset occurs.

HD (Hard Disk Activity) LED

The CCD-CALYPSO offers a LED, marked as HD (placed within the front panel). This LED signals activity on any device attached to the SATA or the IDE ports.

GP (General Purpose) LED

A second, programmable LED can be also observed from the front panel. The status of the GP LED is controlled by the GPO18 output of the ICH6. Setting this pin to 1 will switch on the LED. As of current, the GP LED is not dedicated to any particular hardware or firmware function (this may change in the future).

Hot Swap Detection

The *CompactPCI* specification added the signal ENUM# to the PCI bus to allow the board hot swapping. This signal is routed to the GPI3 of the ICH6. A System Management Interrupt (SMI) can be requested if ENUM# changes by insertion or removal of a board.

Note that the CCD-CALYPSO itself is not a hot swap device, because it makes no sense to remove the system controller from a *CompactPCI* system. However, it is capable to recognize the hot swap of peripheral boards and to start software that is doing any necessary system reconfiguration.

Power Supply Status (DEG#, FAL#)

Power supply failures may be detected before the system crashes down by monitoring the signals DEG# or FAL#. These active low lines are additions of the *CompactPCI* specification and may be driven by the power supply. DEG# signals the degrading of the supply voltages, FAL# there possible failure. On the CCD-CALYPSO the signal FAL# is routed to the GPI4 and DEG# to the GPI5 of the ICH6.

PXI Trigger Signals

As an option, the CCD-CALYPSO supports four of the eight trigger signals of the PXI standard, as defined by National Instruments. The trigger signals are provided by the local SIO (Super-I/O) chip IT8761E. GPIO20/21 are routed to TRIG0/1, and GPIO26/27 are used to control TRIG6/7. These signals can also be used as GPIO lines in a non-PXI environment.

Local GPIO Option

In addition to the GPIO / PXI-Trigger lines optionally available on J2, the expansion connector PEXP provides another two GPIO lines available for user specific application. The 5V TTL signals sio_gpio16/17 are controlled by the on-board SIO IT8761E, with an internal 50kΩ PU resistor and capable of sinking 24mA each.

Rear I/O Options

Optionally, the CCD-CALYPSO can be used for rear I/O with respect to the following functions:

- Analog Graphics
- 1 Gigabit Ethernet Port
- 3 SATA Ports
- 3 USB Ports
- Keyboard, Mouse
- COM1 (TTL Level)

The analog graphics and the gigabit ethernet port 1 signals are routed to multiplexers on the CCD-CALYPSO. These switches, controlled by BIOS, select either the front panel or the rear I/O connection. The COM1 port does not include the physical transceiver (TTL level only). This transceiver is located on the rear I/O module CCT-RIO instead. Each of the above functions can be activated individually (by appropriate stuffing/removing of resistor networks).

The CCD CPU card by default is suitable for a 64-bit *CompactPCI* backplane. However, the J2/P2 pin assignments of a 64-bit CPCI backplane differ substantially from a *CompactPCI* rear I/O backplane. Hence [usage of the rear I/O features is available only as stuffing options on the CCD CPU board, which have to be ordered explicitly.](#)

[The system in use must be equipped with a P2 *CompactPCI* rear I/O backplane.](#) If the system is provided with a P2 *CompactPCI* 64-bit backplane instead, several of the CCD rear I/O signals will collide with the 64-bit address/data lines on the backplane, with unpredictable results regarding the rear I/O signal integrity.



Single Slot Rear I/O Backplane EKF Part No. 932.4.01.000

Installing and Replacing Components

Before You Begin

Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect any telecommunication links, networks or procedures described in this chapter. Failure links before you open the system or perform or equipment damage. Some parts of the the power switch is in its off state.



the system from its power source and from modems before performing any of the to disconnect power, or telecommunication any procedures can result in personal injury system can continue to operate even though

Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a some ESD protection by wearing an metal part of the system chassis or board original ESD protected packaging. Retain the antistatic box) in case of returning the board to EKF for rapair.



station is not available, you can provide antistatic wrist strap and attaching it to a front panel. Store the board only in its original packaging (antistatic bag and

Installing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related *CompactPCI* slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighbored front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return



Removing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Identify the board, be sure to touch the board only at the front panel
- unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighbored front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only



Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.





EMC Recommendations

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Reccomended Accessories

| | | |
|-------------------------|--------------------------------------|--|
| Blind CPCI Front Panels | EKF Elektronik | Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP |
| Ferrit Bead Filters | ARP Datacom, 63115 Dietzenbach | Ordering No. 102 820 (cable diameter 6.5mm) 102 821 (cable diameter 10.0mm) 102 822 (cable diameter 13.0mm) |
| Metal Shielding Caps | Conec-Polytronic, 59557 Lippstadt | Ordering No. CDFA 09 165 X 13129 X (DB9) CDSFA 15 165 X 12979 X (DB15) CDSFA 25 165 X 12989 X (DB25) |

Installing or Replacing the Memory Modules

Note: If you decide to replace the memory, observe the precautions in 'Before You Begin'

By default, the CCD-CALYPSO comes fully equipped and tested with two DDR2 SD-RAM memory modules. So normally there should be no need to install the memory modules.

The CCD-CALYPSO requires at least one PC2-3200/4200 (400/533MHz) DDR2 SDRAM SO-DIMM module, for better performance two SO-DIMMs of equal capacity are recommended. Further it is highly recommended that Serial Presence Detect (SPD) SO-DIMMs be used, since this allows the chipset to accurately configure the memory settings for optimum performance.

A replacement memory module must match the 200-pin SO-DIMM form factor (known from Notebook PCs), DDR2, $V_{CC}=1.8V$, PC2-3200/PC2-4200 (400/533MHz), on-die termination (ODT), unbuffered, non-ECC style. Suitable modules are available up to 1GB. The i915GM supports modules of up to a maximum of 14 address lines (A0...A13). Memory modules organized by more than 14 address lines are not suitable.

Replacement of the Battery

When your system is turned off, a battery maintains the voltage to run the time-of-day clock and to keep the values in the CMOS RAM. The battery is rechargeable and should last during the lifetime of the CCD-CALYPSO. For replacement, the old battery must be desoldered, and the new one soldered. We suggest that you send back the board to EKF for battery replacement.

Warning

Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type. Do not expose a battery to fire.



Technical Reference

Local PCI Devices

The following table shows the on-board PCI devices and their location within the PCI configuration space. These devices consist of the Ethernet controllers and several devices within the i915GM chip set.

| Bus Number | Device Number | Function Number | Vendor ID | Device ID | Description |
|------------|---------------|-----------------|-----------|-----------|-----------------------------|
| 0 | 0 | 0 | 0x8086 | 0x2590 | Host Bridge |
| 0 | 2 | 0 | 0x8086 | 0x2592 | Internal Graphics Device |
| 0 | 2 | 1 | 0x8086 | 0x2792 | Int. Graphics Config. Regs. |
| 0 | 27 | 0 | 0x8086 | 0x2668 | Intel High Definition Audio |
| 0 | 28 | 0 | 0x8086 | 0x2660 | PCI Express Port 1 |
| 0 | 28 | 1 | 0x8086 | 0x2662 | PCI Express Port 2 |
| 0 | 28 | 2 | 0x8086 | 0x2664 | PCI Express Port 3 |
| 0 | 28 | 3 | 0x8086 | 0x2666 | PCI Express Port 4 |
| 0 | 29 | 0 | 0x8086 | 0x2658 | USB UHCI Controller #1 |
| 0 | 29 | 1 | 0x8086 | 0x2659 | USB UHCI Controller #2 |
| 0 | 29 | 2 | 0x8086 | 0x265A | USB UHCI Controller #3 |
| 0 | 29 | 3 | 0x8086 | 0x265B | USB UHCI Controller #4 |
| 0 | 29 | 7 | 0x8086 | 0x265C | USB 2.0 EHCI Controller |
| 0 | 30 | 0 | 0x8086 | 0x244E | PCI-to-PCI Bridge |
| 0 | 30 | 2 | 0x8086 | 0x266E | AC'97 Audio Controller |
| 0 | 30 | 3 | 0x8086 | 0x266D | AC'97 Modem Controller |
| 0 | 31 | 0 | 0x8086 | 0x2640 | LPC Bridge |
| 0 | 31 | 1 | 0x8086 | 0x266F | IDE Controller |
| 0 | 31 | 2 | 0x8086 | 0x2651 | SATA Controller |
| 0 | 31 | 3 | 0x8086 | 0x266A | SMB Controller |

| Bus Number | Device Number | Function Number | Vendor ID | Device ID | Description |
|-----------------|---------------|-----------------|-----------|--|-------------------------|
| 3 ¹⁾ | 0 | 0 | 0x8086 | 0x108B ²⁾ 0x109A ²⁾ | Ethernet Controller NC1 |
| 4 ¹⁾ | 0 | 0 | 0x8086 | 0x108B ²⁾ 0x109A ²⁾ | Ethernet Controller NC2 |

¹⁾ This bus number can vary depending on the PCI enumeration schema implemented in BIOS.

²⁾ The CCD-CALYPSO is available with a 82573E (0x108B) or 82573L (0x109A) Ethernet controller.

Local SMB Devices

The CCD-CALYPSO contains a few devices that are reachable via the System Management Bus (SMBus). These are the clock generation chip, the SPD EEPROMs on the SO-DIMM memory modules, a general purpose serial EEPROM and a supply voltage and CPU temperature controlling device in particular. Other devices could be connected to the SMB via the *CompactPCI* signals IPMB SCL (J1 B17) and IPMB SDA (J1 C17).

| Address | Description |
|---------|--|
| 0x58 | Hardware Monitor/CPU Temperature Sensor (LM87) |
| 0xA0 | SPD of SODIMM1 |
| 0xA2 | SPD of SODIMM2 |
| 0xAE | General Purpose EEPROM |
| 0xD2 | Main Clock Generation (CK-410M) |

Hardware Monitor LM87

Located on the SMBus the CCD-CALYPSO offers a hardware monitor of type LM87/NSC. This device is capable to observe board and CPU temperatures as well as several supply voltages generated on the board with a resolution of 8 bit. The following table shows the mapping of the voltage inputs of the LM87 to the corresponding supply voltages of the CCD-CALYPSO:

| Input | Source | Resolution [mV] | Register |
|-------|------------------|-----------------|----------|
| AIN1 | CPU Core Voltage | 9.8 | 0x28 |
| AIN2 | +1.05V | 9.8 | 0x29 |
| VCCP1 | +1.5V | 14.1 | 0x21 |

| Input | Source | Resolution [mV] | Register |
|-----------|--------------------|-----------------|----------|
| VCCP2/D2- | +1.8V | 14.1 | 0x25 |
| +2.5V/D2+ | +2.5V | 13 | 0x20 |
| +3.3V | +3.3V | 17.2 | 0x22 |
| +5V | +5V | 26 | 0x23 |
| +12V | +12V ¹⁾ | 62.5 | 0x24 |

¹⁾ Revision 2 or higher.

Beside the continuous measuring of temperatures and voltages the LM87 may compare these values against programmable upper and lower boundaries. As soon as a measurement violates the allowed value, the LM87 may request an interrupt via the GPI[11] of the ICH6.

GPIO Usage

GPIO Usage ICH6

| CCD-CALYPSO GPIO Usage ICH6 | | | | |
|-----------------------------|------|------|-------------|---|
| GPIO | Type | Tol. | Function | Description |
| GPI 0 | I | 5V | CPCI_REQ6# | CompactPCI Bus Request Line #6 |
| GPI 1 | I | 5V | CPCI_REQ5# | CompactPCI Bus Request Line #5 |
| GPI 2 | I | 5V | CPCI_INTP | CompactPCI Interrupt Request Line INTP |
| GPI 3 | I | 5V | CPCI_ENUM# | CompactPCI System Enumeration Line ENUM# |
| GPI 4 | I | 5V | CPCI_FAL# | CompactPCI Power Failure Line FAL# |
| GPI 5 | I | 5V | CPCI_DEG# | CompactPCI Power Degeneration Line DEG# |
| GPI 6 | I | 3.3V | GP_JUMP# | BIOS CMOS Values Reset Jumper JGP |
| GPI 7 | I | 3.3V | CPCI_SYSEN# | CompactPCI System Slot Enable Line SYSEN# |
| GPI 8 | I | 3.3V | N/A | Not used on CCD (fixed to GND) |
| GPI 9 | I | 3.3V | USB_OC4# | USB Port #4 Overcurrent Detect Line |
| GPI 10 | I | 3.3V | USB_OC5# | USB Port #5 Overcurrent Detect Line |
| GPI 11 | I | 3.3V | HM_INT# | Hardware Monitor LM87 Interrupt Line |
| GPI 12 | I | 3.3V | EXP_PME# | Expansion Interface PME# Line |
| GPI 13 | I | 3.3V | EXP_SMI# | Expansion Interface SMI# Line |

| CCD-CALYPSO GPIO Usage ICH6 | | | | |
|-----------------------------|------|-------|--------------|--|
| GPIO | Type | Tol. | Function | Description |
| GPI 14 | I | 3.3V | N/A | Not used on CCD (fixed to GND) |
| GPI 15 | I | 3.3V | N/A | Not used on CCD (fixed to GND) |
| GPO 16 | O | 3.3V | CPCI_GNT6# | CompactPCI Bus Grant Line #6 |
| GPO 17 | O | 3.3V | CPCI_GNT5# | CompactPCI Bus Grant Line #5 |
| GPO 18 | O | 3.3V | GP_LED | General Purpose LED Control (via PLD) |
| GPO 19 | O | 3.3V | N/A | Not used on CCD |
| GPO 20 | O | 3.3V | PLD_SCL | Local Option Reg Interface (within PLD) |
| GPO 21 | O | 3.3V | PLD_SDA | Local Option Reg Interface (within PLD) |
| GPO 23 | O | 3.3V | CPCI_INTS_EN | Connect SERIRQ to CompactPCI Line INTS LOW: SERIRQ disconnected from INTS HIGH: SERIRQ connected to INTS |
| GPIO 24 | O | 3.3V | CPCI_SMB_EN | Connect CPCI IPMB to local SMBus LOW: IPMB disconnected from SMBus HIGH: IPMB connected to SMBus |
| GPIO 25 | O | 3.3V | CPCI_CLK_EN | Enable CompactPCI Clock Buffer |
| GPI 26 | I | 3.3V | N/A | Not used on CCD (fixed to GND) |
| GPIO 27 | O | 3.3V | VGA_SWITCH | VGA Switching Line: LOW: VGA via Rear I/O HIGH: VGA via Front I/O |
| GPIO 28 | O | 3.3V | ETH_SWITCH | Ethernet Switching Line: LOW: Ethernet Port #1 via Rear I/O HIGH: Ethernet Port #1 via Front I/O |
| GPI 29-31 | I | 3.3V | BOARD_CFG | Board Configuration Jumpers |
| GPIO 32 | O | 3.3V | NC1_EN | Enable Ethernet Controller NC1 |
| GPIO 33 | O | 3.3V | NC2_EN | Enable Ethernet Controller NC2 |
| GPIO 34 | I/O | 3.3V | N/A | Not used on CCD |
| GPI 40 | I | 5V | CPCI_REQ4# | CompactPCI Bus Request Line #4 |
| GPI 41 | I | 3.3V | LPC_DRQEXP# | Expansion Interface LPC DMA Request Line |
| GPO 48 | O | 3.3V | CPCI_GNT4# | CompactPCI Bus Grant Line #4 |
| GPO 49 | OD | 1.05V | CPU_PWRGD | CPU Power Good Line |

GPIO Usage FWH

| CCD-CALYPSO GPIO Usage FWH | | | | | | | | | | | | | | | | | | | |
|----------------------------|-------|------|-------------|---|-------|-------|------|---|---|---|---|---|---|---|---|---|---|---|----|
| GPIO | Type | Tol. | Function | Description | | | | | | | | | | | | | | | |
| GPI 0 | I | 3.3V | FWH_ID | FWH Identity: Fixed to GND (indicates FWH #1) | | | | | | | | | | | | | | | |
| GPI 1 | I | 3.3V | IDE_CLBID# | IDE 80pol. Cable Detection Line | | | | | | | | | | | | | | | |
| GPI 2 | I | 3.3V | WDOGRST | Last Hardware Reset caused by watchdog | | | | | | | | | | | | | | | |
| GPI 3 | I | 3.3V | LSB PCB REV | <table border="1"> <thead> <tr> <th>GPI 4</th> <th>GPI 3</th> <th>Rev.</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>2</td> </tr> <tr> <td>1</td> <td>1</td> <td>3+</td> </tr> </tbody> </table> | GPI 4 | GPI 3 | Rev. | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 2 | 1 | 1 | 3+ |
| GPI 4 | GPI 3 | Rev. | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | | | | | | | | | | | | | | | | | |
| 1 | 0 | 2 | | | | | | | | | | | | | | | | | |
| 1 | 1 | 3+ | | | | | | | | | | | | | | | | | |
| GPI 4 | I | 3.3V | MSB PCB REV | | | | | | | | | | | | | | | | |

GPIO Usage SIO

| CCD-CALYPSO GPIO Usage SIO | | | | |
|----------------------------|------|-----------------------|------------|---|
| GPIO | Type | Tol. | Function | Description |
| GPIO 13 | I | 5V ¹⁾ | CPCI_64EN# | CompactPCI 64-Bit Backplane |
| GPIO 14/15 | I/O | 5V/8mA ¹⁾ | N/A | Not used on CCD |
| GPIO 16 | I/O | 5V/24mA ¹⁾ | SIO_GPIO16 | GPIO on Expansion Interface PEXP Pin 29 |
| GPIO 17 | I/O | 5V/24mA ¹⁾ | SIO_GPIO17 | GPIO on Expansion Interface PEXP Pin 30 |
| GPIO 20 | I/O | 5V/8mA ¹⁾ | PXI_TRIG0 | PXI Trigger 0 on CompactPCI J2 Pin B16 |
| GPIO 21 | I/O | 5V/8mA ¹⁾ | PXI_TRIG1 | PXI Trigger 1 on CompactPCI J2 Pin A16 |
| GPIO 22-25 | I/O | 5V/24mA ¹⁾ | N/A | Not used on CCD |
| GPIO 26 | I/O | 5V/24mA ¹⁾ | PXI_TRIG6 | PXI Trigger 6 on CompactPCI J2 Pin E18 |
| GPIO 27 | I/O | 5V/24mA ¹⁾ | PXI_TRIG7 | PXI Trigger 7 on CompactPCI J2 Pin E16 |

¹⁾ These GPIOs have pullup resistors of approx. 50kΩ within the SIO.

Configuration Jumpers

Reset Jumper BIOS CMOS RAM Values (JGP)

The jumper JGP is used to bring the contents of the battery backed CMOS RAM to a default state. The BIOS uses the CMOS to store configuration values, e.g. the actual boot devices. Using this jumper is only necessary, if it is not possible to enter the setup of the BIOS. To reset the CMOS RAM mount a jumper on JGP and perform a system reset. As long as the jumper is stuffed the BIOS will use the default CMOS values after any system reset. To get normal operation again, the jumper has to be removed.

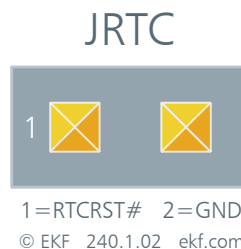


| JGP | Function |
|--------------------------|-------------------------|
| Jumper OFF ¹⁾ | No CMOS reset performed |
| Jumper ON | CMOS reset performed |

¹⁾ This setting is the factory default.

Reset Jumper ICH6 RTC Core (JRTC)

The jumper JRTC is used to reset the battery backed core of the ICH6. This effects some registers within the ICH6 RTC core that are important before the CPU starts its work after a system reset. Note that JRTC will neither perform the clearing of the CMOS RAM values nor resets the real time clock. To reset the RTC core the board must be removed from the system rack. Short-circuit the pins of JRTC for about 1 sec. After that reinstall the board to the system and switch on the power. It is important to accomplish the RTC reset while the board has no power.



| JRTC | Function |
|--------------------------|------------------------|
| Jumper OFF ¹⁾ | No RTC reset performed |
| Jumper ON | RTC reset performed |

¹⁾ This setting is the factory default.

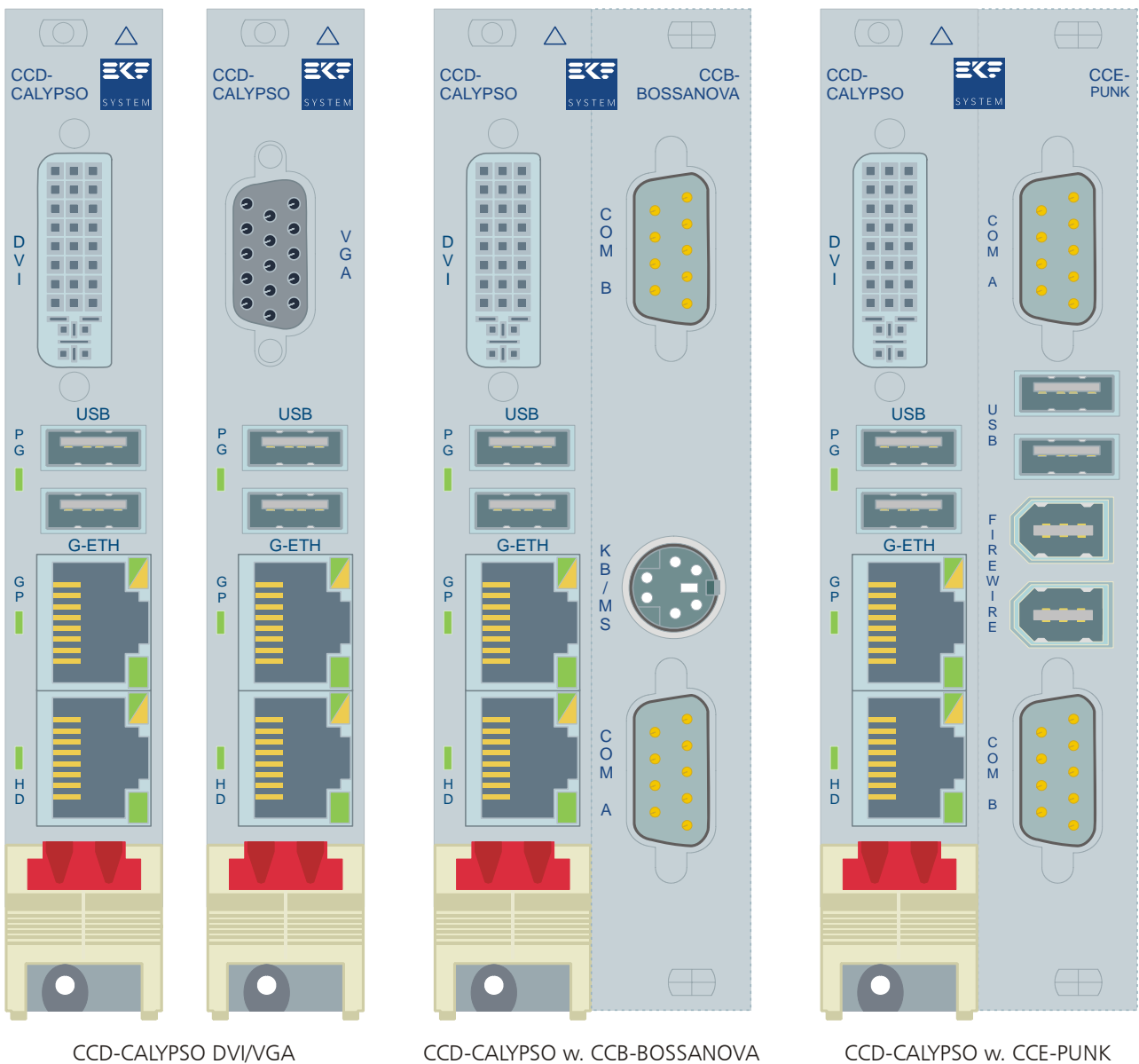
Connectors

Caution

Some of the internal connectors provide operating voltage (3.3V and 5V) to devices inside the system chassis, such as internal peripherals. Not all of these connectors are overcurrent protected. Do not use these internal connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

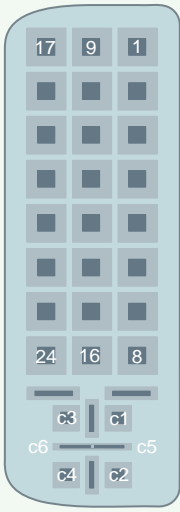
Front Panel Connectors

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Typical CCD-CALYPSO Front Panel Elements

Video Monitor Connector DVI-I

| DVI-I | | | | | | |
|---|----|------|---------------------|-----------------------|---------------------|-----------------------|
|  | 17 | TX0- | 9 | TX1- | 1 | TX2- |
| | 18 | TX0+ | 10 | TX1+ | 2 | TX2+ |
| | 19 | GND | 11 | GND | 3 | GND |
| | 20 | | 12 | | 4 | |
| | 21 | | 13 | | 5 | |
| | 22 | GND | 14 | DDC_POW ¹⁾ | 6 | DDC_SCL ²⁾ |
| | 23 | TXC+ | 15 | GND | 7 | DDC_SDA ²⁾ |
| | 24 | TXC- | 16 | DVI_HP | 8 | VSYNC ²⁾ |
| | | | c3 | BLUE ²⁾ | c1 | RED ²⁾ |
| | | | c6 | GND | c5 | GND |
| | | c4 | HSYNC ²⁾ | c2 | GREEN ²⁾ | |

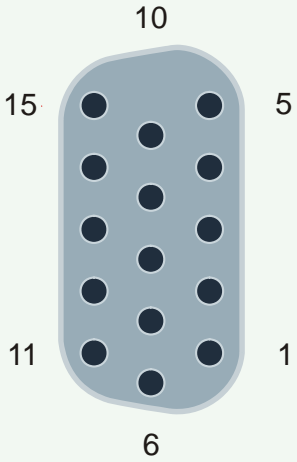
¹⁾ +5V protected by a PolySwitch Fuse 0.75A.

²⁾ This signal may be switched either to the front connector or to the rear I/O adapter CCT-RIO.

For attachment of an ordinary analog RGB monitor to the DVI-I receptacle, there are both adapters and also adapter cables available from DVI-I to the HD-SUB15 connector. Attachment of digital monitors (flat panel displays) should be done by means of a DVI to DVI cable (single link style cable is sufficient).

Video Monitor Connector VGA

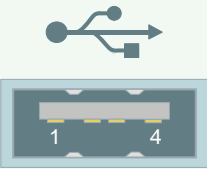
As an option, the CCD-CALYPSO can be equipped with a legacy VGA connector (High-Density D-Sub 15-position female connector). The VGA connector replaces the DVI-I receptacle, and the digital video interface therefore is not available with this option.

| VGA (Option) | | |
|--|----|-----------------------|
|  | 1 | RED ²⁾ |
| | 2 | GREEN ²⁾ |
| | 3 | BLUE ²⁾ |
| | 4 | NC |
| | 5 | GND |
| | 6 | GND |
| | 7 | GND |
| | 8 | GND |
| | 9 | DDC_POW ¹⁾ |
| | 10 | GND |
| | 11 | NC |
| | 12 | DDC_SDA ²⁾ |
| | 13 | HSYNC ²⁾ |
| | 14 | VSYNC ²⁾ |
| | 15 | DDC_SCL ²⁾ |

¹⁾ +5V protected by a PolySwitch Fuse 0.75A

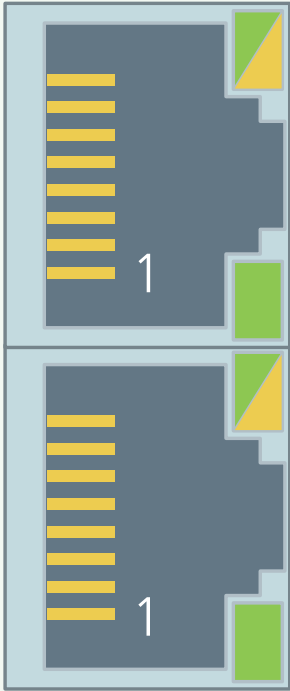
²⁾ This signal may be switched either to the front connector or to the rear I/O adapter CCT-RIO.

USB Connectors

| USB Ports 1/2 | | |
|---|---|-------------------|
|  | 1 | POW ¹⁾ |
| | 2 | USB DATA NEG |
| | 3 | USB DATA POS |
| | 4 | GND |

¹⁾ +5V protected by an Electronic Fuse 0.5A

Ethernet Connectors

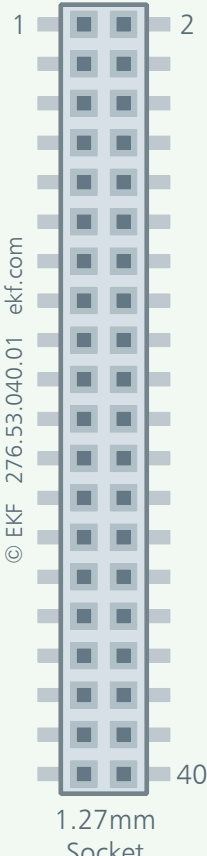
| G-ETH1/2 (RJ45) | | |
|---|---|-------------------------|
|  <p>270.02.08.5</p> | 1 | NC1_MDX0+ ¹⁾ |
| | 2 | NC1_MDX0- ¹⁾ |
| | 3 | NC1_MDX1+ ¹⁾ |
| | 4 | NC1_MDX2+ ¹⁾ |
| | 5 | NC1_MDX2- ¹⁾ |
| | 6 | NC1_MDX1- ¹⁾ |
| | 7 | NC1_MDX3+ ¹⁾ |
| | 8 | NC1_MDX3- ¹⁾ |
| | 1 | NC2_MDX0+ |
| | 2 | NC2_MDX0- |
| | 3 | NC2_MDX1+ |
| | 4 | NC2_MDX2+ |
| | 5 | NC2_MDX2- |
| | 6 | NC2_MDX1- |
| | 7 | NC2_MDX3+ |
| | 8 | NC2_MDX3- |

¹⁾ This signal may be switched either to the front connector or to the rear I/O adapter CCT-RIO.

The upper green/yellow dual-LED signals 1Gbit/s when lit yellow, 100Mbit/s when lit green, and 10Mbit/s when off. The lower green LED indicates LINK established when continuously on, and data transfer (activity) when blinking. If the lower green LED is permanently off, no LINK is established.

Internal Connectors

Expansion Interface Header PEXP

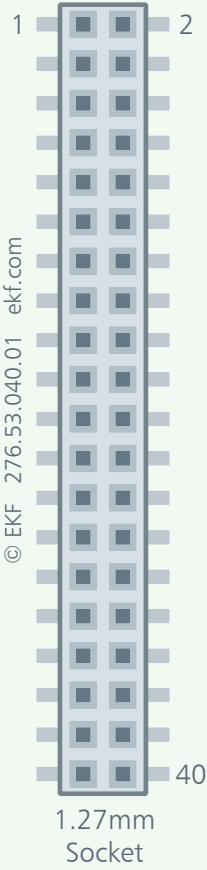
| PEXPT/PEXPB | | | | |
|--|-------------|----|----|----------------------------|
|  | GND | 1 | 2 | +3.3V |
| | PCI_CLK | 3 | 4 | PCI_RST# |
| | LPC_AD0 | 5 | 6 | LPC_AD1 |
| | LPC_AD2 | 7 | 8 | LPC_AD3 |
| | LPC_FRM# | 9 | 10 | LPC_DRQ# |
| | GND | 11 | 12 | +3.3V |
| | SERIRQ | 13 | 14 | EXP_PME# |
| | EXP_SMI# | 15 | 16 | SIO_CLK14 |
| | FWH_ID0 | 17 | 18 | FWH_INIT# |
| | ICH_RCIN# | 19 | 20 | ICH_A20GATE |
| | GND | 21 | 22 | +5V |
| | USB_EXP_P2- | 23 | 24 | USB_EXP_P1- |
| | USB_EXP_P2+ | 25 | 26 | USB_EXP_P1+ |
| | USB_EXP_OC# | 27 | 28 | H_DBRESET# |
| | SIO_GPIO16 | 29 | 30 | SIO_GPIO17 |
| | GND | 31 | 32 | +5V |
| | AC97_SDOUT | 33 | 34 | AC97_SDIN0 |
| | AC97_RST# | 35 | 36 | AC97_SYNC |
| | AC97_BITCLK | 37 | 38 | AC97_SDIN1 |
| | SPEAKER | 39 | 40 | +12V/+VCCRTC ¹⁾ |

¹⁾ This pin is connected to +12V via a 0-ohm jumper (default on rev. 2 or higher). Alternatively it connects to +VCCRTC via a diode (default on revision 0 or 1 boards).

The expansion interface header is available on both sides of the board, top and bottom, in order to provide attachment of the CCA-LAMBADA either to the left or to the right side of the CCD-CALYPSO.

WARNING: Neither the +3.3V pin, nor the +5V pin, nor the +12V pin are protected against a short circuit situation! This connector therefore should be used only for attachment of an expansion board like CCA-LAMBADA. The maximum current flowing across these pins should be limited to 2A per power rail.

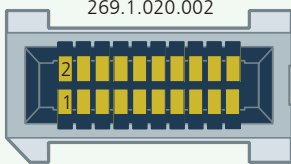
ATA/IDE Header PIDE

| PIDET/PIDEB | | | | |
|--|------------------|----|----|------------|
|  | IDE_RST# | 1 | 2 | GND |
| | IDE_D07 | 3 | 4 | IDE_D08 |
| | IDE_D06 | 5 | 6 | IDE_D09 |
| | IDE_D05 | 7 | 8 | IDE_D10 |
| | IDE_D04 | 9 | 10 | IDE_D11 |
| | IDE_D03 | 11 | 12 | IDE_D12 |
| | IDE_D02 | 13 | 14 | IDE_D13 |
| | IDE_D01 | 15 | 16 | IDE_D14 |
| | IDE_D00 | 17 | 18 | IDE_D15 |
| | GND | 19 | 20 | +3.3V |
| | IDE_DREQ | 21 | 22 | +3.3V |
| | IDE_IOW# | 23 | 24 | GND |
| | IDE_IOR# | 25 | 26 | GND |
| | IDE_IORDY | 27 | 28 | +5V |
| | IDE_DACK# | 29 | 30 | +5V |
| | IDE_IRQ (INT 15) | 31 | 32 | GND |
| | IDE_A1 | 33 | 34 | IDE_CBLID# |
| | IDE_A0 | 35 | 36 | IDE_A2 |
| | IDE_CS1# | 37 | 38 | IDE_CS3# |
| | IDE_ACT# | 39 | 40 | GND |

Like the expansion interface header the IDE connector is also available on both sides of the board.

WARNING: Neither the +3.3V pin, nor the +5V pin are protected against a short circuit situation! This connector therefore should be used only for attachment of the C10-CFA adapter or an expansion board like CCA-LAMBADA. The maximum current flowing across these pins should be limited to 2A per power rail.

PCI Express Expansion Header PPCIE

| PPCIE | | | | |
|---|---------|----|----|----------|
|  <p>269.1.020.002</p> <p>PCI Express High Speed Socket Connector</p> | GND | 1 | 2 | GND |
| | +5V | 3 | 4 | +3.3V |
| | +5V | 5 | 6 | +3.3V |
| | GND | 7 | 8 | GND |
| | PE_CLKP | 9 | 10 | PE_RST# |
| | PE_CLKN | 11 | 12 | PE_WAKE# |
| | GND | 13 | 14 | GND |
| | PE_1TP | 15 | 16 | PE_1RP |
| | PE_1TN | 17 | 18 | PE_1RN |
| | GND | 19 | 20 | GND |

The PCI Express expansion interface header is available on the top side of the board.

WARNING: Neither the +3.3V pin, nor the +5V pin are protected against a short circuit situation! The maximum current flowing across these pins should be limited to 2A per power rail.

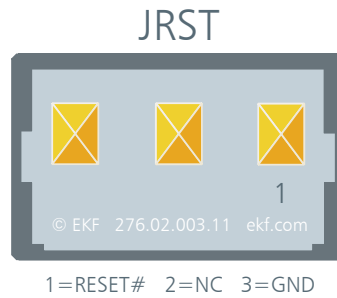
Speaker Header JSPK



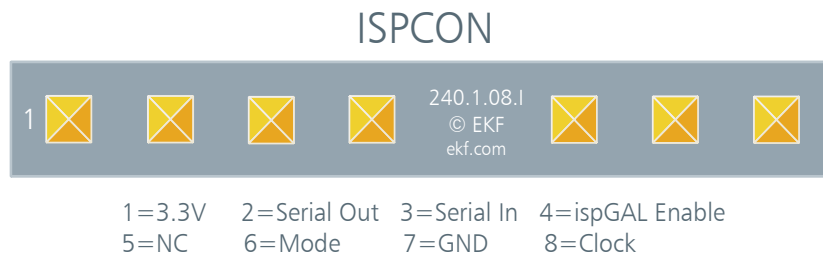
WARNING: The +5V pin is protected against a short circuit situation by a 0.1A PolySwitch. The JSPK connector should be used exclusively for direct attachment of a dynamic speaker device. When connecting to the input of a sound card, most likely a short-circuit situation will occur between the +5V pin of the JSPK connector and the GND pin of the audio-card input, which could cause permanent damage to the CCD-CALYPSO and the audio board, despite the PolySwitch resettable fuse. A workaround to this would be to place a 1k resistor across pin 1 and pin 2 of the JSPK connector, and strapping a single wire cable from JSPK pin 2 to the audio input.

System Reset Header JRST

The jumper JRST is used to perform a manually system reset. By default JRST is connected with a short cable to a micro switch located within the front panel handle. The switch performs a system reset by short-circuiting the pins 1 and 3 of JRST.



PLD Programming Header ISPCON



Note: The ISPCON is not stuffed. Its footprint is situated at the bottom side of the board.

Processor Debug Header PITP

| PITP | |
|------|-----------------|
| 1 | TDI |
| 2 | TMS |
| 3 | TRST# |
| 4 | NC |
| 5 | TCK |
| 6 | NC |
| 7 | TDO |
| 8 | BCLKN |
| 9 | BCLKP |
| 10 | GND |
| 11 | FBO |
| 12 | RST# |
| 13 | BPM5# |
| 14 | GND |
| 15 | BPM4# |
| 16 | GND |
| 17 | BPM3# |
| 18 | GND |
| 19 | BPM2# |
| 20 | GND |
| 21 | BPM1# |
| 22 | GND |
| 23 | BPM0# |
| 24 | DBA# |
| 25 | DBR# |
| 26 | VTAP |
| 27 | V _{TT} |
| 28 | V _{TT} |

Note: The Debug Header is situated at the bottom side of the board.

CompactPCI J1

| #J1 | A | B | C | D | E |
|-----|------------------------|------------------------|------------------------|---------------------|----------------------|
| 25 | 5V | REQ64# ²⁾ | ENUM# ¹⁾ | 3.3V | 5V |
| 24 | AD1 | 5V | V(I/O) | AD0 | ACK64# ²⁾ |
| 23 | 3.3V | AD4 | AD3 | 5V | AD2 |
| 22 | AD7 | GND | 3.3V | AD6 | AD5 |
| 21 | 3.3V | AD9 | AD8 | M66EN ³⁾ | C/BE0# |
| 20 | AD12 | GND | V(I/O) | AD11 | AD10 |
| 19 | 3.3V | AD15 | AD14 | GND | AD13 |
| 18 | SERR# ¹⁾ | GND | 3.3V | PAR | C/BE1# |
| 17 | 3.3V | IPMB SCL ⁴⁾ | IPMB SDA ⁴⁾ | GND | PERR# ¹⁾ |
| 16 | DEVSEL# ¹⁾ | GND | V(I/O) | STOP# ¹⁾ | LOCK# ¹⁾ |
| 15 | 3.3V | FRAME# ¹⁾ | IRDY# ¹⁾ | GND | TRDY# ¹⁾ |
| 14 | KEY AREA | | | | |
| 13 | | | | | |
| 12 | | | | | |
| 11 | AD18 | AD17 | AD16 | GND | C/BE2# |
| 10 | AD21 | GND | 3.3V | AD20 | AD19 |
| 9 | C/BE3# | GND ⁵⁾ | AD23 | GND | AD22 |
| 8 | AD26 | GND | V(I/O) | AD25 | AD24 |
| 7 | AD30 | AD29 | AD28 | GND | AD27 |
| 6 | REQ# ¹⁾ | GND | 3.3V | CLK | AD31 |
| 5 | BRSVP1A5 ⁵⁾ | BRSVP1B5 ⁵⁾ | RST# | GND | GNT# |
| 4 | IPMB PWR | GND | V(I/O) | INTP ¹⁾ | INTS ¹⁾ |
| 3 | INTA# ¹⁾ | INTB# ¹⁾ | INTC# ¹⁾ | 5V | INTD# ¹⁾ |
| 2 | TCK ⁵⁾ | 5V | TMS ⁵⁾ | TDO ⁵⁾ | TDI ⁵⁾ |
| 1 | 5V | -12V | TRST# ⁵⁾ | +12V | 5V |

¹⁾ This pin is pulled up with 1kΩ to V(I/O). Other pull up resistor values (e.g. 2.7kΩ for V(I/O)=+3.3V) are available on request.

²⁾ This pin is not used on CCD-CALYPSO, but pulled up with 1kΩ to V(I/O). Other pull up resistor values on request.

³⁾ This pin is fixed to GND on CCD-CALYPSO to force 33MHz operation since 66MHz operation is not supported.

⁴⁾ This pin is pulled up with 2.4k to J1 pin A4.

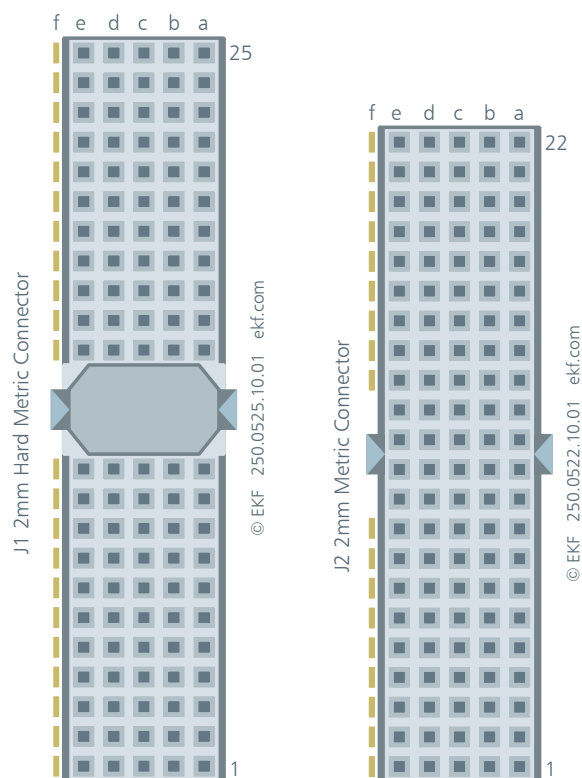
⁵⁾ This pin is not connected.

CompactPCI J2

| #J2 | A | B | C | D | E |
|-----|---|---|---------------------------------|---------------------------------|---|
| 22 | GA4 ⁵⁾ | GA3 ⁵⁾ | GA2 ⁵⁾ | GA1 ⁵⁾ | GA0 ⁵⁾ |
| 21 | CLK6 | GND | RSV NC1_MX2- | RSV NC1_MX3- | RSV NC1_MX3+ |
| 20 | CLK5 | GND | RSV NC1_MX2+ | GND | RSV NC1_MX0+ |
| 19 | GND | GND | RSV NC1_MX1- | RSV NC1_MX1+ | RSV NC1_MX0- |
| 18 | BRSVP2A18 VGA_RED | BRSVP2B18 VGA_GREEN | BRSVP2C18 VGA_HSYNC | GND | BRSVP2E18 PXI_TRIG6 ³⁾ VGA_VSYNC |
| 17 | BRSVP2A17 VGA_BLUE | GND | PRST# ¹⁾ | REQ6# ¹⁾ | GNT6# |
| 16 | BRSVP2A16 PXI_TRIG1 ³⁾ +VCCRTC ⁸⁾ | BRSVP2B16 PXI_TRIG0 ³⁾ DDC_SCL ²⁾ | DEG# ¹⁾ | GND | BRSVP2E16 PXI_TRIG7 ³⁾ DDC_SDA ²⁾ |
| 15 | BRSVP2A15 | GND | FAL# ¹⁾ | REQ5# ¹⁾ | GNT5# |
| 14 | AD35 ¹⁾ SATA_2RN | AD34 ¹⁾ SATA_2RP | AD33 ¹⁾ SATA_ACT# | GND | AD32 ¹⁾ GND |
| 13 | AD38 ¹⁾ GND | GND | V(I/O) | AD37 ¹⁾ SATA_2TP | AD36 ¹⁾ SATA_2TN |
| 12 | AD42 ¹⁾ SATA_1RN | AD41 ¹⁾ SATA_1RP | AD40 ¹⁾ | GND | AD39 ¹⁾ GND |
| 11 | AD45 ¹⁾ GND | GND | V(I/O) | AD44 ¹⁾ SATA_1TP | AD43 ¹⁾ SATA_1TN |
| 10 | AD49 ¹⁾ SATA_ORN | AD48 ¹⁾ SATA_ORP | AD47 ¹⁾ | GND | AD46 ¹⁾ GND |
| 9 | AD52 ¹⁾ GND | GND | V(I/O) | AD51 ¹⁾ USB_P7P | AD50 ¹⁾ USB_P7N |
| 8 | AD56 ¹⁾ SATA_OTN | AD55 ¹⁾ SATA_OTP | AD54 ¹⁾ GND | GND COM1_DSR# | AD53 ¹⁾ COM1_TXD |
| 7 | AD59 ¹⁾ COM1_DTR# | GND COM1_CTS# | V(I/O) COM1_RXD | AD58 ¹⁾ COM1_RTS# | AD57 ¹⁾ COM1_DCD# |
| 6 | AD63 ¹⁾ USB_P3P | AD62 ¹⁾ USB_P3N | AD61 ¹⁾ USB_P4P | GND USB_OC34# | AD60 ¹⁾ USB_P4N |
| 5 | C/BE5# ¹⁾ +5V/1.5A ⁴⁾ | GND (64EN#) ¹⁾ | V(I/O) | C/BE4# ¹⁾ MS_DATA | PAR64 ¹⁾ MS_CLK |
| 4 | V(I/O) | BRSVP2B4 ⁶⁾ +5V/1.5A ⁴⁾ | C/BE7# ¹⁾ KB_DATA | GND | C/BE6# ¹⁾ KB_CLK |

| #J2 | A | B | C | D | E |
|-----|------|------|----------------------|---------------------|---------------------|
| 3 | CLK4 | GND | GNT3# | REQ4# ¹⁾ | GNT4# |
| 2 | CLK2 | CLK3 | SYSEN# ⁷⁾ | GNT2# | REQ3# ¹⁾ |
| 1 | CLK1 | GND | REQ1# ¹⁾ | GNT1# | REQ2# ¹⁾ |

- 1) This pin is pulled up with 1kΩ to V(I/O). Other pull up resistor values (e.g. 2.7kΩ for V(I/O)=+3.3V) are available on request.
- 2) This pin is pulled up via a QuickSwitch with 2.7kΩ to +5V.
- 3) This pin is pulled up with 10kΩ to +5V.
- 4) This pin is protected by a resettable PolySwitch fuse.
- 5) This pin is not connected.
- 6) This pin is connected only in the rear I/O configuration.
- 7) This pin is pulled up with 10kΩ to +3.3V.
- 8) This pin is connected to VCCRTC via a diode.
- 9) Pin positions printed blue: Rear I/O options.



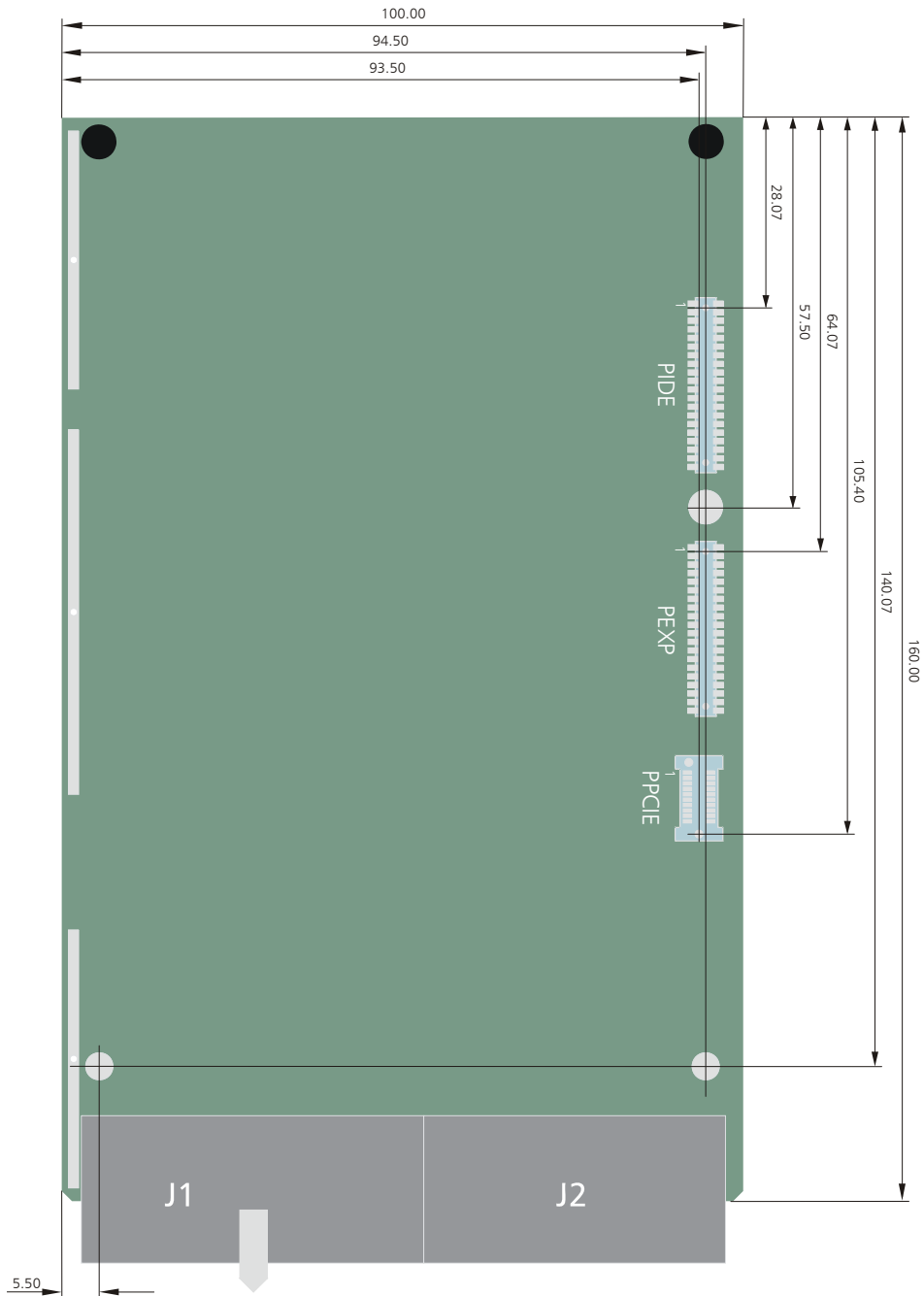
Literature

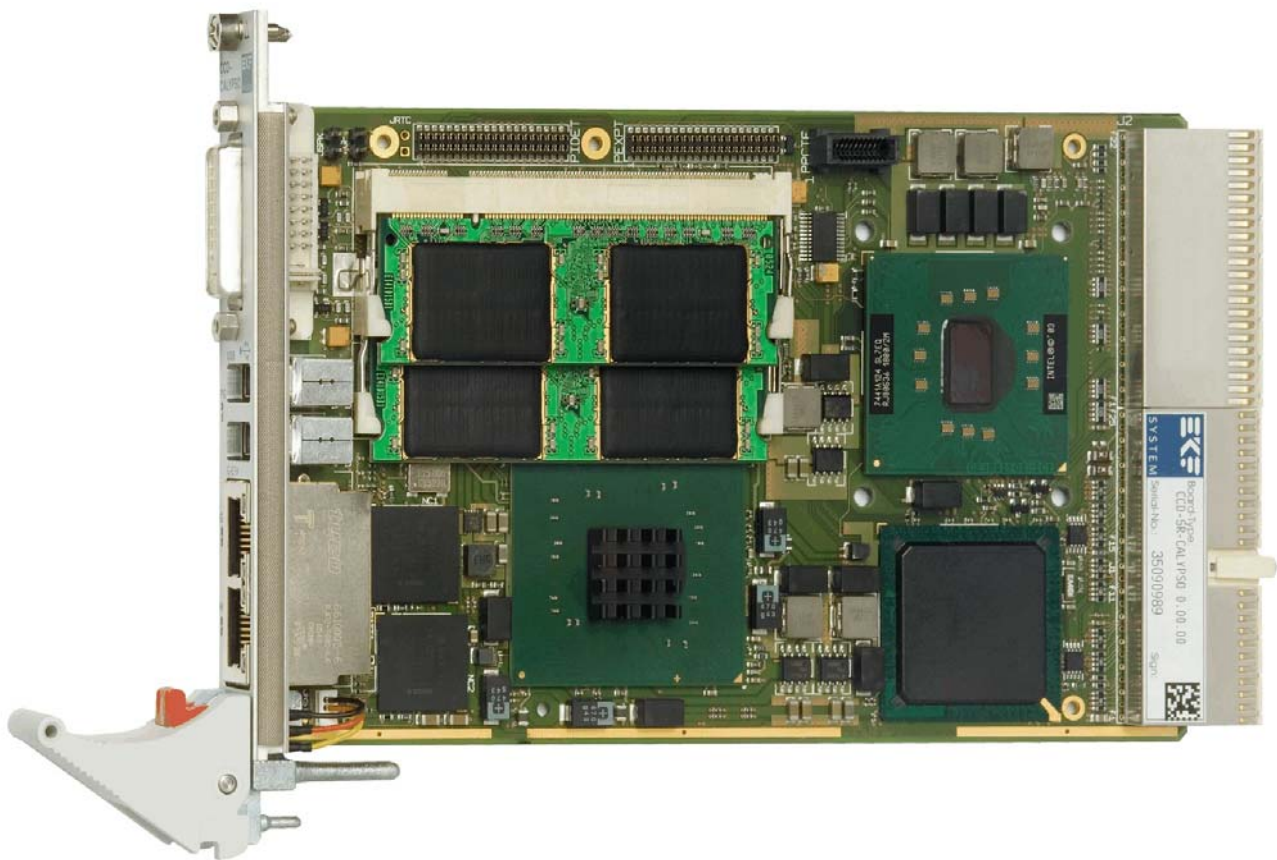
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| <i>CompactPCI</i> | <i>CompactPCI</i> Specification, PICMG 2.0 R3.0, Oct. 1, 1999 | www.picmg.org |
| PCI Express | PCI Express® Base Specification 1.1 | www.pcisig.com |
| PCI Local Bus | PCI 2.2/2.3/3.0 Standards PCI SIG | www.pcisig.com |
| Ethernet | IEEE Std 802.3, 2000 Edition | standards.ieee.org |
| USB | Universal Serial Bus Specification | www.usb.org |
| CompactFlash | CF+ and CompactFlash Specification Revision 3.0 | www.compactflash.org |

Appendix

Mechanical Drawings

The following drawing shows the positions of mounting holes and expansion connectors on the CCD-CALYPSO.





Top View CCD-CALYPSO Shown w/o Heatsink

EKF Elektronik GmbH
Philipp-Reis-Str. 4
59065 HAMM
Germany



Fax. +49 (0)2381/6890-90
Tel. +49 (0)2381/6890-0
Internet www.ekf.com
E-Mail info@ekf.com