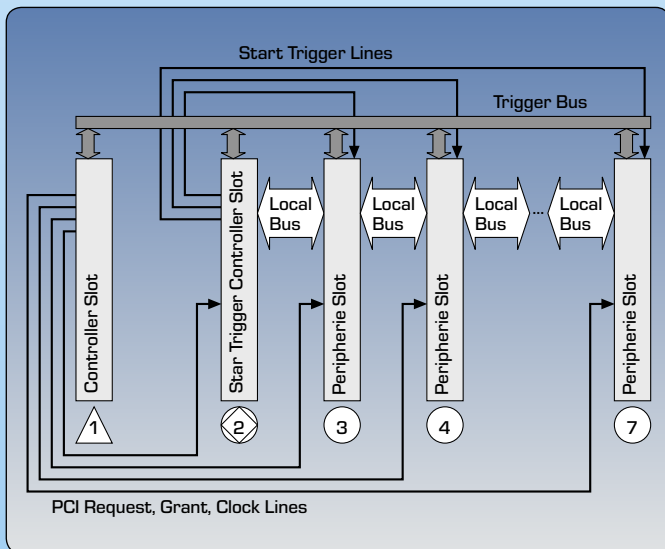
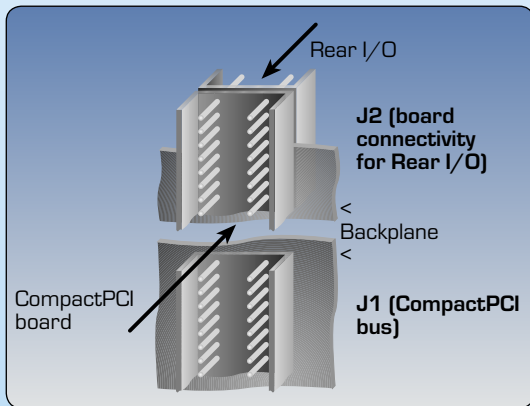
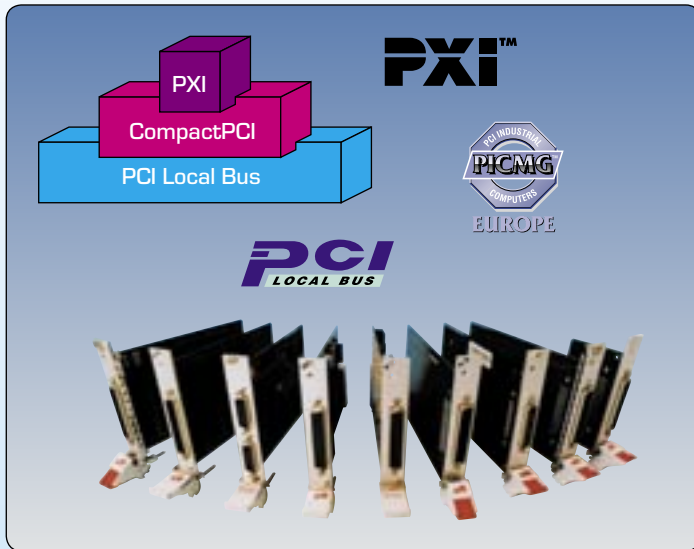


Extended PXI Trigger and Synchronisation

PCI → CompactPCI → PXI



PCI

The PCI standard (Peripheral Component Interconnect) was introduced in 1991 and is implemented in most of the PCs available today.

CompactPCI - "PCI for Industrial Applications"

The CompactPCI standard is based on an expansion of the PCI standard by the PICMG consortium (PCI Industrial Computer Manufacturers Group). The aim of this expansion was to make the PCI bus suitable for industrial applications:

- Robust, mechanic constructions (bus connectors, mounting/ejection mechanisms, board guide rails etc.)
- Standardisation (standard 3 U Europa card form factor, second form factor: 6 U).
- Connectivity from chassis front panel or, with Rear I/O, from chassis back panel.
- Expandability: Backplanes with multiple slots.
- Upgradability: Passive backplane and exchangeable CPU modules in CompactPCI board format.

CompactPCI chassis are available as 19" rack-mount devices or as desktop housings. Passive backplanes are used, with Rear I/O if required (i. e. I/O connectivity via connector J2, no I/O connectors on the front panel). J1 and J2 (J2 only for Rear I/O) are 110-pin 2 mm IEC 1076-4-101 Bellcore male connectors. The CompactPCI bus has a bus width of 32 bit (optional 64 bit) at 33 MHz and a data throughput of 132 MB/s and/or Burst 265 MByte/s. The CPU module is plugged into the very right slot.

PXI - "Extended CompactPCI"

PXI (PCI Extension for Instrumentation, www.pxisa.org) adds the following definitions of synchronisation functions to PCI/CompactPCI:

- **Trigger Bus:** 8 lines, connected to every slot of a PXI bus segment. Used TTL signals like trigger or clock.
- **Star Trigger Bus:** Group of 13 bidirectional lines. They connect slot 2 (Star Trigger Controller Slot) with each of the 13 slots in the primary and secondary bus segment. Used to exchange triggers between slot 2 and other slots with minimum delay.
- **Local Bus:** Group of 13 lines each. They connect each slot with the right and left neighbour slot (right and left bus independent from each other). For TTL or analog signals.
- **10 MHz TTL Clock:** Synchronisation clock delivered by the backplane for all slots.

These signals added to CompactPCI by PXI are wired to connector J2. Connector J1 is the same as on CompactPCI boards. That's the reason, why **CompactPCI boards** that only have the bus connector J1 (i. e. no Rear I/O!) can normally be used in **PXI-Systems**. The additional PXI trigger and synchronisation functions can of course not be used for these boards. The CPU module is plugged into the very left slot of a PXI system chassis.

Specifications	PCI	CompactPCI	PXI
Bus Width	32, 64	32, 64	8, 16, 32, 64.
Timing/Synchronisation	Manufacturer specific	Manufacturer specific	Defined lines
Board Size	Manufacturer specific	3 U standard Europa card 100 mm x 160 mm or 6 U double Europa card 233 mm x 160 mm	3 U standard Europa card 100 mm x 160 mm.
Slots	Depending on PC, often 3 - 4; use of bridges for more slots	Standard 8 slots; use of bridges for more slots	Standard 8 slots, use of bridges for more slots.
Expandability		Bridges	
Applications	Home, office, labs...	Labs, industry, telecom...	Labs, industry...