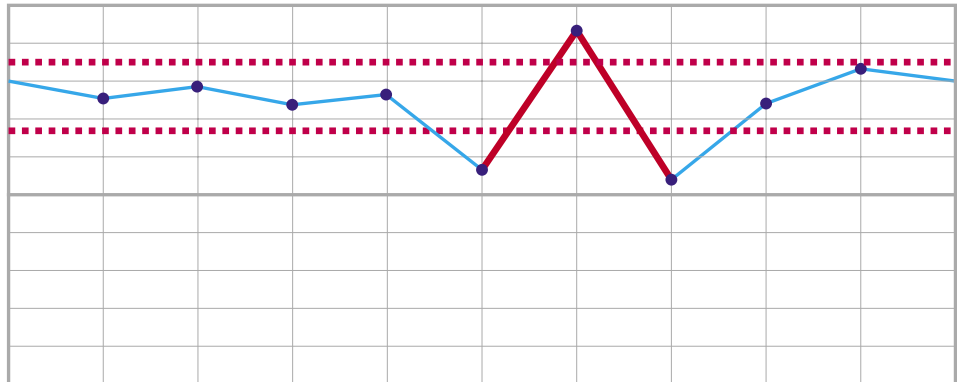
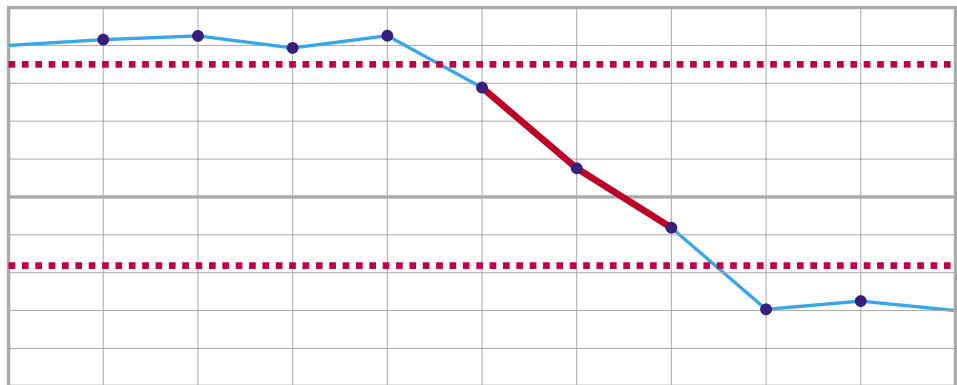




- **Detecting faults of a DC voltage using the option “Window, inside” (“Single-Shot”/“Run” state)**

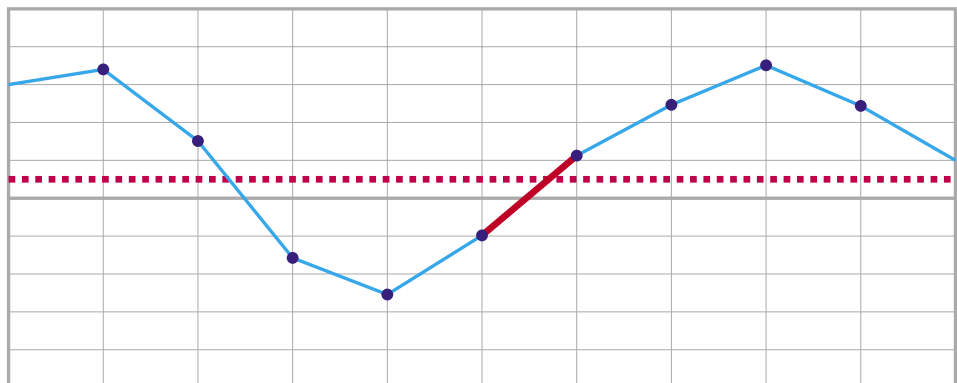


- **Detecting a “forbidden range” eg. in digital technology (“Single-Shot”/“Run” state)**

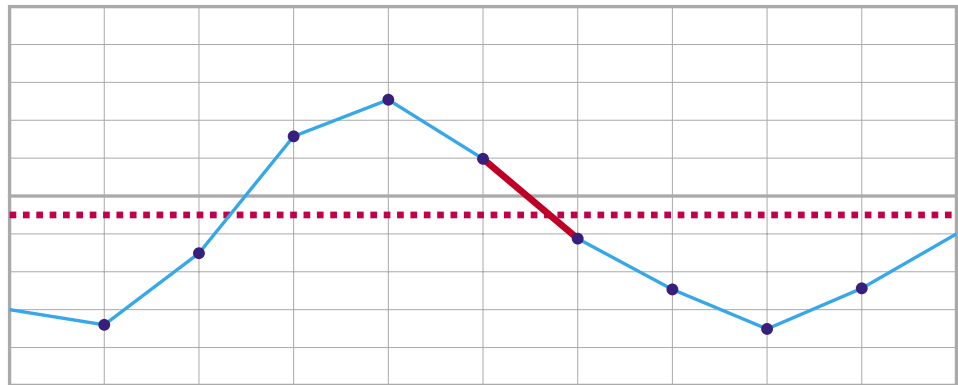


**Edge, rising/edge, falling** In this mode the oscilloscope reacts to a positive or negative deviation of a given threshold. It is similar to the „Level“ triggered mode, but requires the signal to cross the threshold. A static signal does not generate a trigger event. **The edge triggered mode is useful for repetitive AC signals to get a still graph.**

- **Visualising the rising edge (“Run” state)**



- **Visualising the falling edge (“Run” state)**



**Slope, positive/Slope, negative**

This trigger mode is made for very special cases of dynamic signals. It is nearly independent of the absolute voltage. Only the variation of the signal is relevant. If it increases or decreases faster than defined, a trigger event occurs.

The slope is given in voltage per sample time. The voltage is given in volts. The sample time is just implicitly given and must be calculated by the quotient of Time/Memory Depth.

$$\frac{dU}{dt} = \frac{U[V] \cdot \text{Memory}[\text{Samples}]}{t_{\text{Time Base}}[s]}$$

or

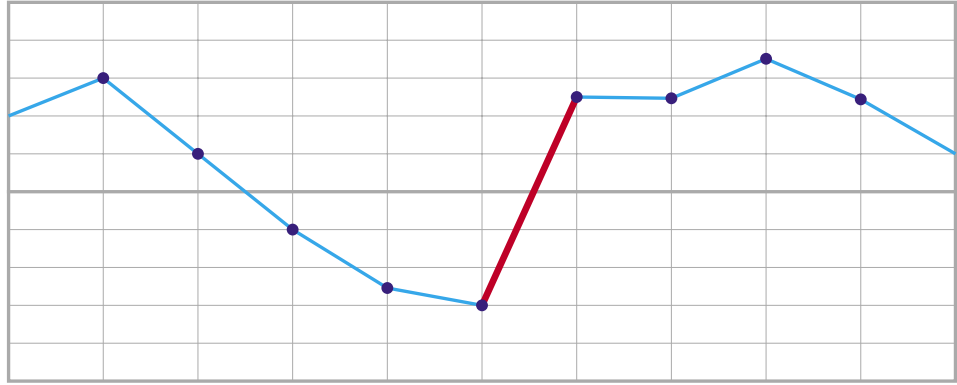
$$U[V] = \frac{dU}{dt} \cdot \frac{t_{\text{Time Base}}[s]}{\text{Memory}[\text{Samples}]}$$

Checking the slope is important for two areas of application. The first one is process control in chemistry, biology and so on. In these applications even great shifts can be normal. However, a sudden great increase signals an error. On the other hand, a frequency measurement can be realized with this mode.

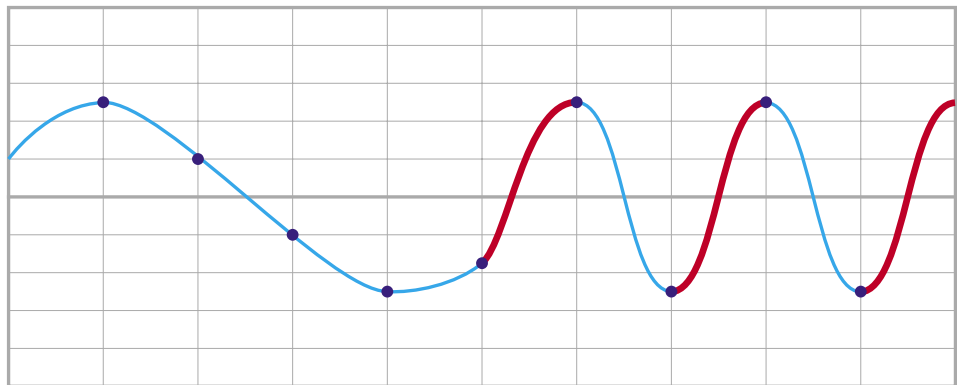
The MEphisto Scope has a limited voltage range. Slopes near the upper or lower limits could exceed the maximum range. Due to this limitation, such a trigger event would then go by unrecognized. To prevent this failure, the trigger also occurs, if the current value plus slope would exceed full scale.

For experimental determination of a useful setting, first choose small values. If you have a signal of 50 Hz and 10...18 V<sub>pp</sub> for example, and a short burst with the same voltage and 1 kHz, use a trigger value of 0.15625 V. The higher the difference of the frequencies, the more likely you will detect the higher one.

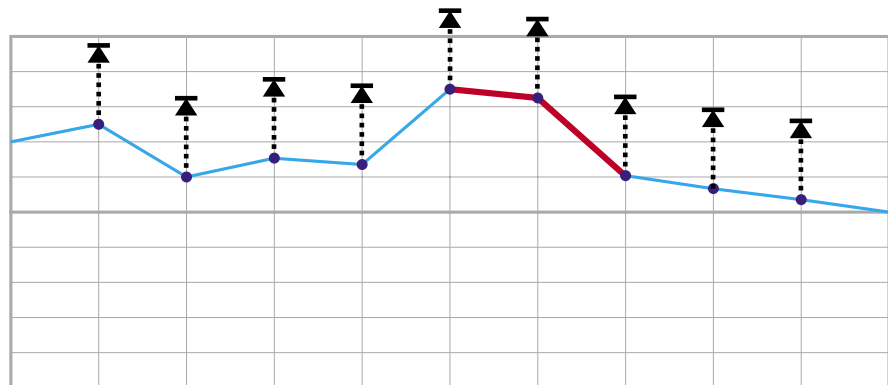
- **Detecting a critical state (“Single-Shot”/“Run” state)**



- **Detecting a frequency (“Run” state)**

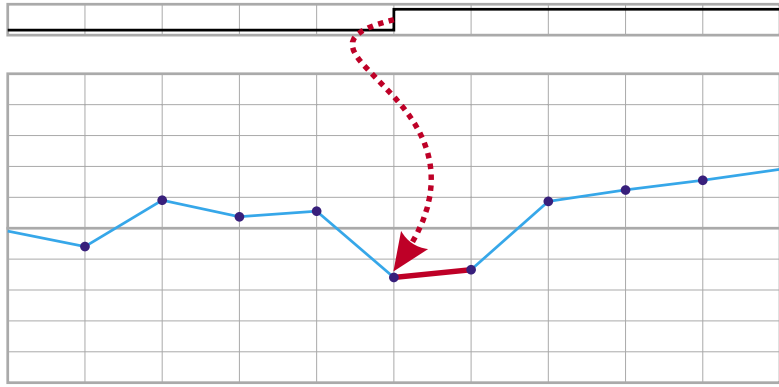


- **Probably exceeding the measurement range with the next value (“Single-Shot”/“Run” state)**



#### **External, rising/External, falling**

In this mode, which is similar to the edge trigger, a rising or falling edge is necessary. However, in this case the trigger source is the digital signal at D23 (pin 26 of the 26-pin D-sub female connector), not one of the analog channels. Like the analog edge trigger, only a logical edge triggers measurement. A static signal will be ignored. The external trigger may be used for synchronization purposes with other devices. Please check the trigger source for compatibility with the MEphisto Scope. Most modern signal generators provide a 5 V-CMOS-level signal which may be used for synchronization.



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## Trigger Modes of the Digital Modules Logic Analyser and Digital Data Logger

### Manual

This trigger mode is used for continuous measurement. It starts immediately after pressing the Run or Single button.

### Pattern

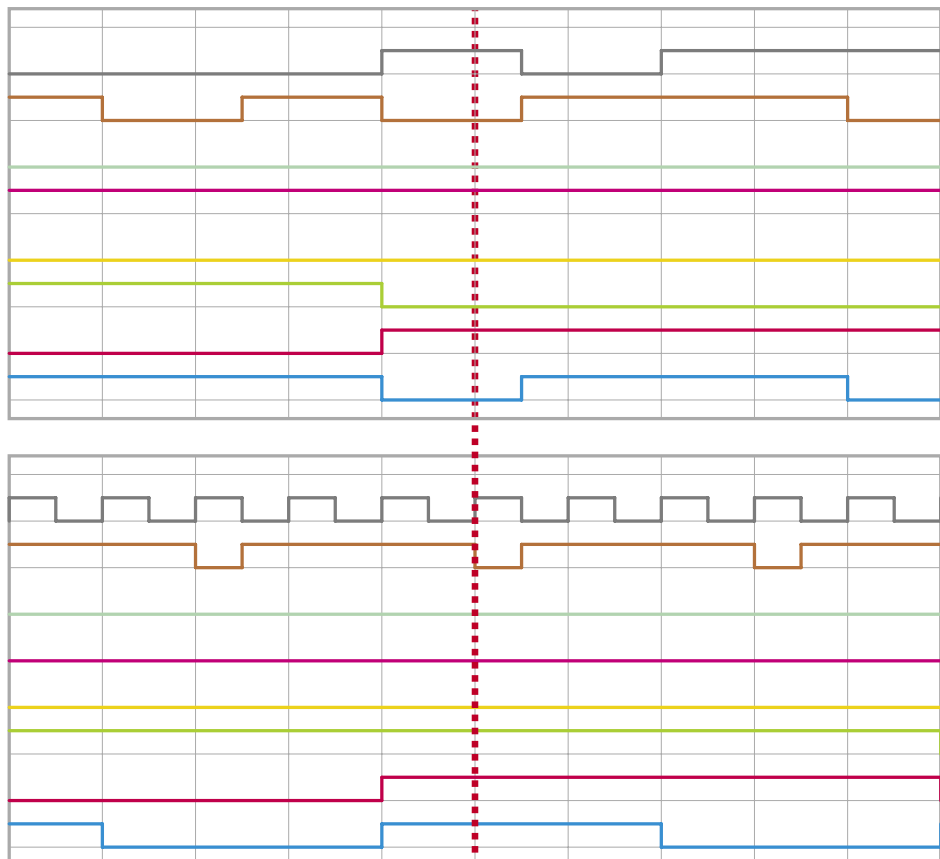
In this mode the logic analyser triggers on the occurrence of the chosen pattern of the lower 8 bits. One single bit can have the following states:

- X: The bit will be ignored.
- 0: At the moment of the trigger event the bit must represent a logical 0.
- 1: At the moment of the trigger event the bit must represent a logical 1.
- F: At the moment of the trigger event the bit must have a falling edge.
- R: At the moment of the trigger event the bit must have a rising edge.

A failsafe trigger criterion is normally made of a combination of several discrete triggers. Here are some examples: Let's say, you want to analyse a memory transaction of a processor. Channel 7 is chosen to be the clock signal, active at rising edge. Channel 6 shows the write impulse that is active on falling edge. The next channels numbered 5 thru 0 will be address lines. The upper eight channels represent the data bits and do not affect the trigger

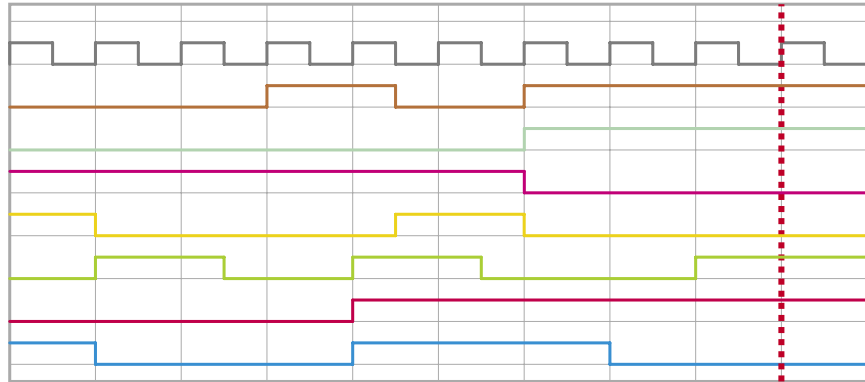
If you want to find out what is written on memory location 7hex (000111bin) you have to select a trigger pattern of RF000111. The channels 8 thru 15 show you the corresponding data on the bus. In this example it is 10010010bin (92hex). Furthermore you can see that setup and hold times are presumably met.

For this example please note, that it just works for very slow microcontrollers or processors capable of single cycle operation.



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You may test a state machine or sequencer on whether or not it will enter a forbidden state by selecting this state as the trigger pattern. In the following example let's assume that this trigger pattern is R1100110. The clock edge should be used to reliably find the state itself and not some asynchronous switching between two other states. The history on the left of the trigger event informs you about how the error occurred.



These two examples, being as different as they could, were chosen to show you how powerful this kind of pattern trigger can be. Nevertheless, always keep in mind, that a combination of uncorrelated signals will have poor success with triggering. Seen from this angle the number of relevant channels should be as low as possible. On the other hand, the lower the criteria are the more false trigger events you get. You have to decide what tradeoffs are acceptable to yield maximal failsafe events.

#### **External, rising/External, falling**

In this mode, which is similar to the edge trigger, a rising or falling edge is necessary. However, in this case the trigger source is the digital signal at D23 (pin 26 of the 26-pin D-sub female connector). Similar to the edge trigger, only a logical edge triggers measurement. A static signal will be ignored. The external trigger may be used for synchronization purposes with other devices. Please check the trigger source for compatibility with the MEphisto Scope. Most modern signal generators provide a 5 V-CMOS-level signal which may be used for synchronization.

