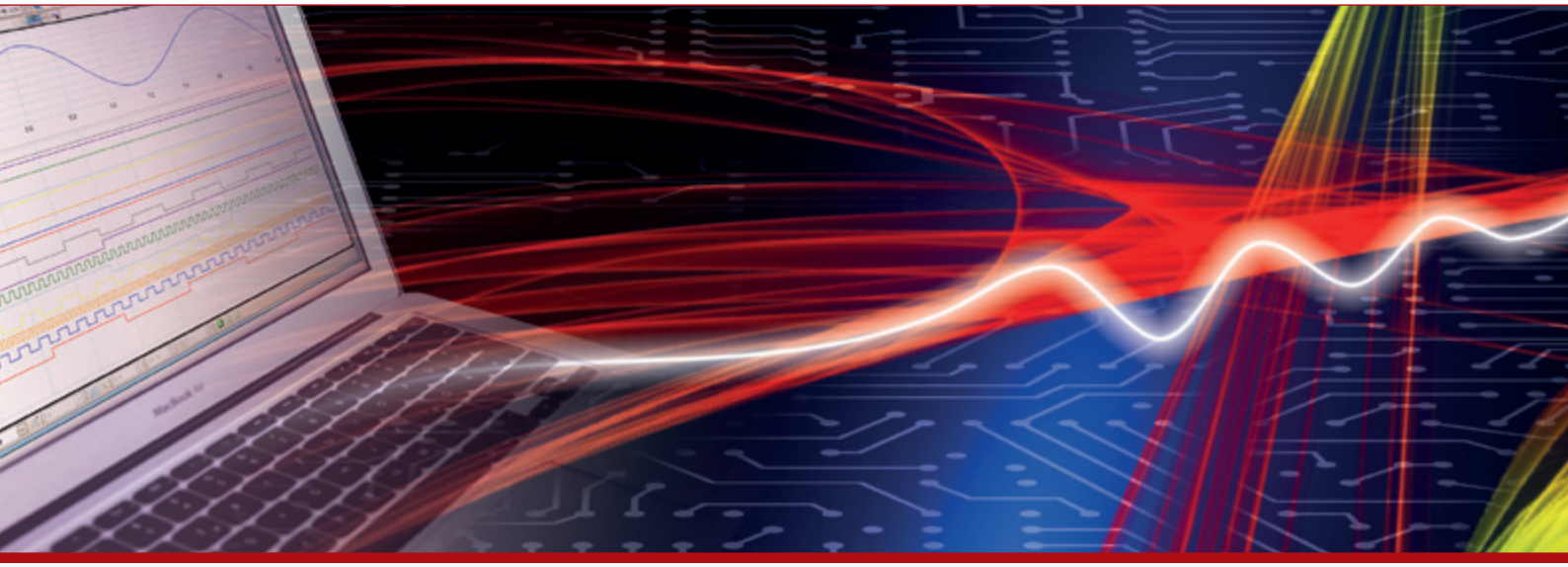
Product Datasheet - Technical Specifications



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Specifications

Analog Input Specifications

Table 28 lists the specifications for the analog input subsystem on the DT9826 Series modules.

Table 28: Analog Input Specifications

Feature	Specifications
Number of analog input channels DT9826: DT9826-4: DT9826-8:	 16 single-ended, simultaneous 4 single-ended, simultaneous 8 single-ended, simultaneous
ADC Type	Delta-Sigma converter per channel
Resolution	24 bits
Range	±10 V
Gain	1
Throughput per channel	41.666 kHz
System accuracy, to % of FSR @ 20 kHz System accuracy, to % of FSR @ 41.666 kHz	±0.01% ±0.015%
Data encoding	Offset binary
Coupling	DC
Input voltage	±11 V maximum
Maximum input voltage (without damage) Power on: Power off:	 ±30 V ±20 V
Input impedance	10 MΩ Series 2 kΩ ,1000 pf Filter
Input bias current	±20 nA
Nonlinearity 20 kHz 40 kHz	 ±3 LSB ±5 LSB
Inherent quantizing error	0.5 LSB
Drift Zero: Gain:	 ±10 µV per °C ±30 ppm per °C
Differential linearity drift (of FSR/° C)	±2 ppm
Monotonicity	1 LSB
ESD protection Arc: Contact:	 8 kV 4 kV
Reference	+1.250 V (internal)

Table 28: Analog Input Specifications (cont.)

Feature	Specifications
–3 dB Frequency	A/D sample frequency * 0.216
Effective Number of Bits (ENOB)[a] (Sampling at 40 kHz with a 1 kHz sine wave at –0.37 dB below full-scale (IBF))	14.1 bits
Signal-to-noise plus distortion (SINAD)	86.48 dB

a. ENOB = (SINAD – 1.76 – IBF)/6.02. Refer to page 110 for more information about ENOBs.

Measuring Dynamic Performance

FFT plots show the dynamic performance of the DT9826 Series. Many users believe that a 24-bit A/D device provides 24-bit accuracy or at least close to that accuracy. But, when measuring a dynamic signal (with frequency components above DC), factors such as noise, harmonic distortion, and phase shift (particularly at low bandwidths), as well as the accuracy of the signal generator itself, degrade the accuracy of the measurement.

Layout of the critical circuit etch, spacing between noise-generating and noise-sensitive devices as well as analog and digital etch patterns, and thermal effects from one circuit to another are all culprits in degrading accuracy. Through careful design, these effects are minimized.

DC specifications are useful. When measuring a 0 V input signal, you can see the system's base-line noise. Under these conditions, the DT9826 Series yields the highest ENOB (Effective Number of Bits) value of 16 bits. Figure 26A shows the FFT plot when measuring a 0 V signal with a 40 kHz sample frequency. Figure 26A shows the FFT plot when measuring a 0 V signal with a 20 kHz sample frequency.

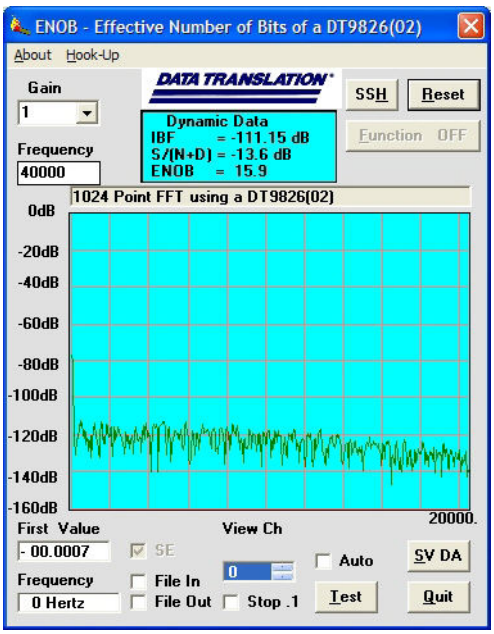

Figure 26A. ENOB of 15.9 bits when measuring a 0 V signal with a 40 kHz sample frequency

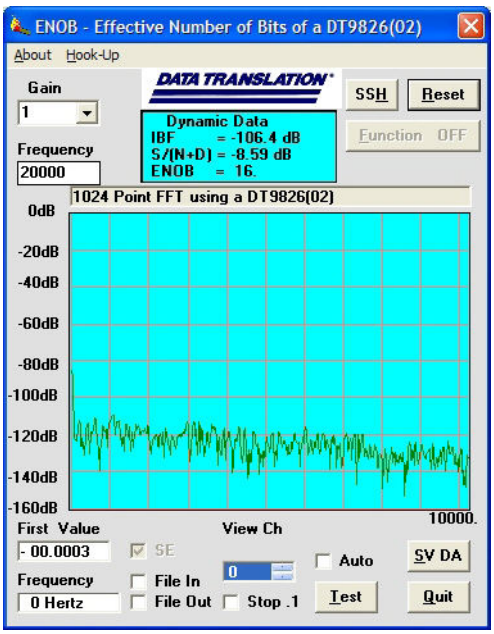

Figure 26B. ENOB of 16 bits when measuring a 0 V signal with a 20 kHz sample frequency

Figure 26: ENOB Value When Measuring a 0 V Input Signal

Dynamic FFT plots at higher input voltages and operating frequencies give the best indicator of accuracy under real-world conditions. For example, when measuring a ±5 V, 1 kHz sine wave (a signal at 1/2 full-scale or –6 dB), the DT9826 Series can achieve ENOB values of 15 bits. Figure 27A shows the FFT plot when measuring a ±5 V, 1 kHz sine wave with a 40 kHz sample frequency; Figure 27B shows the FFT plot when measuring a ±5 V, 1 kHz sine wave with a 20 kHz sample frequency.

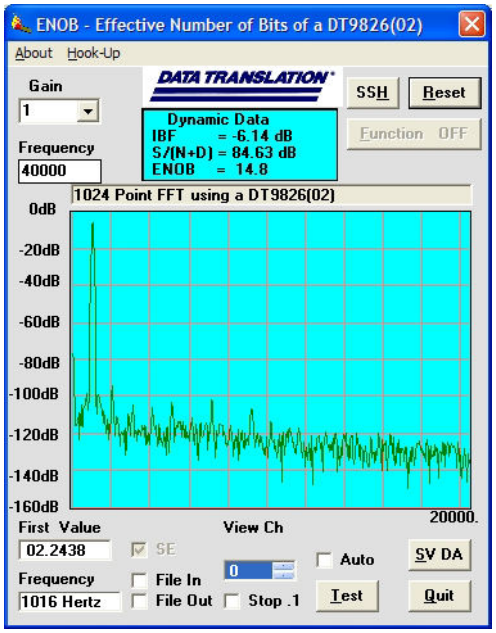

Figure 27A. ENOB of 14.8 bits when measuring a ±5 V, 1 kHz signal with a 40 kHz sample frequency

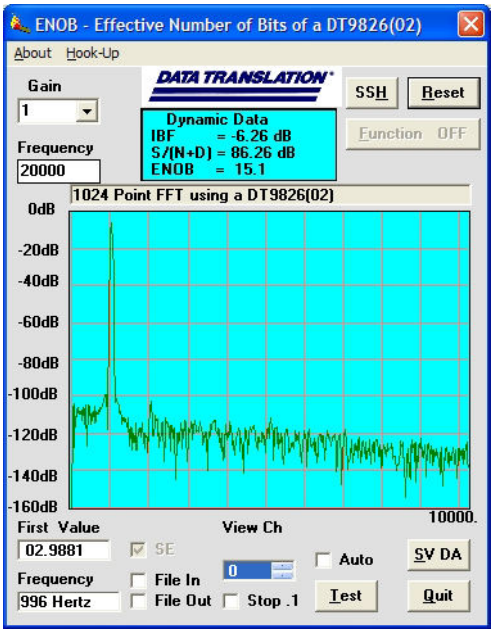

Figure 27B. ENOB of 15.1 bits when measuring a ±5 V, 1 kHz signal with a 20 kHz sample frequency

Figure 27: ENOB Value When Measuring a 1/2 Full-Scale (–6 dB) Input Signal

The ENOB value further degrades at the maximum input signal voltage (full-scale) and the fastest throughput frequency. Under these conditions, the DT9826 Series yields an ENOB value of 14.3 bits; you can see the full range of the A/D without distortion at the peaks. Figure 28A shows the FFT plot when measuring a ±10 V, 1 kHz sine wave with a 40 kHz sample frequency. Figure 28B shows the FFT plot when measuring a ±10 V, 1 kHz sine wave with a 20 kHz sample frequency.

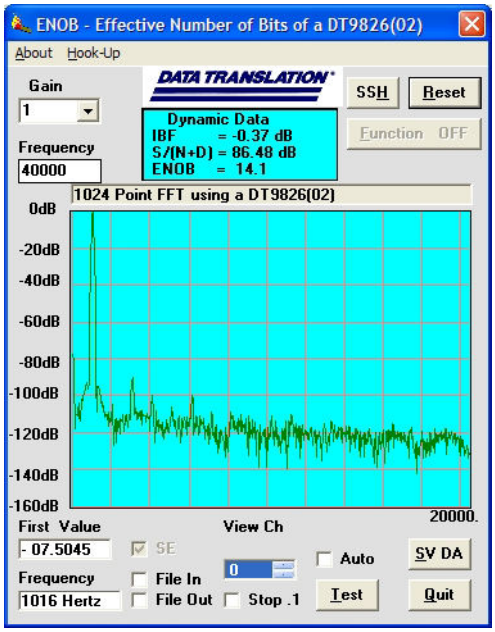

Figure 28A. ENOB of 14.1 bits when measuring a ±10 V, 1 kHz sine wave with a 40 kHz sample frequency

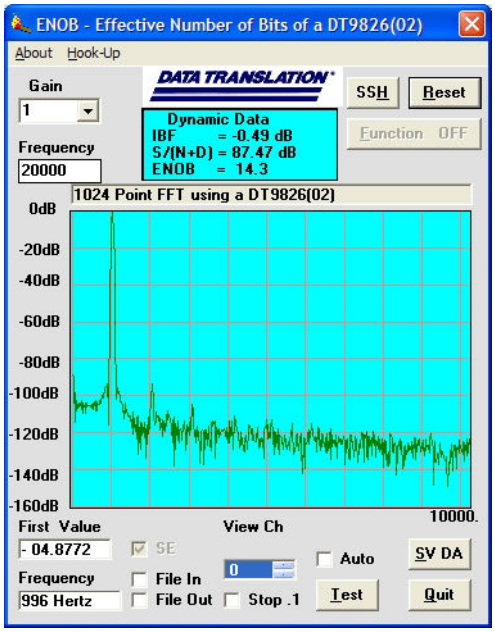

Figure 28B. ENOB of 14.3 bits when measuring a ±10 V, 1 kHz sine wave with a 20 kHz sample frequency

Figure 28: ENOB Value When Measuring a Full-Scale Input Signal

Conditions of use determine the accuracy of dynamic measurements. While ENOB values can be higher when you measure input signals that are less than full-scale, the results may be misleading for many users. ENOB values at full-scale and at the full throughput of the device give the best indicator of accuracy under real-world conditions.

Digital I/O Specifications

Table 29 lists the specifications for the digital I/O subsystems on the DT9826 Series modules.

Table 29: Digital I/O Specifications

Feature	Specifications
Number of digital I/O lines	16 (8 in, 8 out)
Number of ports	2 (8 bits each)
Logic family	LVTTL (5 V tolerant)
Logic sense	Positive true
Inputs Input type: Input logic load: High input voltage: Low input voltage: Low input current: Termination:	 Level-sensitive 1 LVTTL 2.0 V minimum 0.8 V maximum 0.4 mA maximum Inputs tied to +5 V through 22 kΩ pullup resistors
Outputs High output: Low output: High output current: Low output current:	 3.84 V minimum 0.33 V maximum –2 mA maximum 6 mA maximum
Interrupt on change	No
Clocked with sample clock	Yes
Software I/O selectable	No

Counter/Timer Specifications

Table 30 lists the specifications for the counter/timer subsystem on the DT9826 Series modules.

Table 30: Counter/Timer Specifications

Feature	Specifications
Number of channels	2
Resolution	32 bits per channel
Logic family	LVTTL (5 V tolerant)
Inputs Input logic load: High input voltage: Low input voltage: Low input current:	 1 LVTTL 2.0 V minimum 0.8 V maximum –0.4 mA maximum
Outputs High output: Low output: High output current: Low output current:	 2.0 V minimum 0.8 V maximum –2 mA maximum 8 mA maximum

Tachometer Input Specifications

Table 30 lists the specifications for the tachometer input on the DT9826 Series modules.

Table 31: Tachometer Input Specifications

Feature	Specifications
Number of channels	1
Resolution	31 bits per channel
Input voltage range	±30 V
Threshold voltage	±2 V with 0.5 V hysteresis
Maximum input frequency	1 MHz
Minimum pulse width high/low (minimum amount of time it takes a C/T to recognize an input pulse)	0.4 μs
Clock frequency for tachometer measurements	12 MHz (83 ns resolution)

External Trigger Specifications

Table 32 lists the specifications for the external A/D trigger on the DT9826 Series modules.

Table 32: External A/D Trigger Specifications

Feature	Specifications
Trigger sources Internal: External:	 Software-initiated Software-selectable
Input type	Edge-sensitive
Logic family	LVTTL (5 V tolerant)
Inputs Input logic load: Input termination: High input voltage: Low input voltage: Low input current:	 1 LVTTL 22 kΩ pull-up to +3.3 V 2.0 V minimum 0.8 V maximum –0.25 mA maximum
Minimum pulse width High: Low:	 500 ns 500 ns
Triggering modes Single scan: Continuous scan:	 Yes Yes

Internal Clock Specifications

Table 33 lists the specifications for the internal A/D clock on the DT9826 Series modules.

Table 33: Internal A/D Clock Specifications

Feature	Specifications
Reference frequency	48 MHz
A/D master clock frequency range	0.011176 Hz to 16 MHz
A/D clock frequency	(Master Clock Frequency/6)/64
–3 dB frequency	A/D Clock Frequency * 0.216

Power, Physical, and Environmental Specifications

Table 34 lists the power, physical, and environmental specifications for the DT9826 Series modules.

Table 34: Power, Physical, and Environmental Specifications

Feature	Specifications
Power, +5 V	±5% @ 500 mA maximum
Dimensions OEM: BNC:	 8.230 inches x 3.937 inches x 0.753 inches 209.04 mm x 100 mm x 19.13 mm 8.500 inches x 4.170 inches x 1.968 inches 215.9 mm x 105.92 mm x 50 mm
Weight OEM: BNC:	 0.294 lbs (133.4 g) 1.949 lbs (884.4 g)
Environmental Operating temperature range: Storage temperature range: Relative humidity: Altitude:	 0° C to 55° C –25° C to 85° C to 95%, noncondensing to 10,000 feet

Mating Connector Specifications

Table 35 lists the mating cable connectors for the connectors on the DT9826 Series modules.

Table 35: Mating Cable Connectors

Module/Panel	Connector	Part Number on Module (or Equivalent)	Mating Cable Connector
BNC connection box	Analog input	AMP/Tyco AMP 5747375-8	AMP/Tyco 5-747917-2
	Digital In/Out	AMP/Tyco 5747301-8	AMP/Tyco 5-747916-2
	Cntr/Timer, Analog Out, Clk/Trig	AMP/Tyco 5747301-8	AMP/Tyco 5-747916-2
OEM version	J2	AMP/Tyco 6-104068-8	AMP/Tyco 3-111196-4[a]
	J3	AMP/Tyco 6-104068-8	AMP/Tyco 3-111196-4[a]
EP353 accessory panel	J1	AMP/Tyco 5102321-6	AMP/Tyco 1658622-6
	J2	AMP/Tyco 5747375-8	AMP/Tyco 5-747917-2
EP356 accessory panel	J1	AMP/Tyco 5747301-8	AMP/Tyco 5-747916-2
	J2	AMP/Tyco 5747301-8	AMP/Tyco 5-747916-2

a. The mating PCB receptacle is AMP/Tyco 6-104078-3.

Regulatory Specifications

The DT9826 Series modules are CE-compliant. Table 36 lists the regulatory specifications for the DT9826 Series modules.

Table 36: Regulatory Specifications

Feature	Specifications
Emissions (EMI)	FCC Part 15, Class A EN55011:2007 (Based on CISPR-11, 2003/A2, 2006)
Immunity	EN61326-1:2006 Electrical Equipment for Measurement, Control, and Laboratory Use EMC Requirements EN61000-4-2:2009 Electrostatic Discharge (ESD) 4 kV contact discharge, 8 kV air discharge, 4 kV horizontal and vertical coupling planes EN61000-4-3:2006 Radiated electromagnetic fields, 3 V/m, 80 to 1000 MHz; 3 V/m, 1.4 GHz to 2 GHz; 1 V/m, 2 GHz to 2.7 GHz EN61000-4-4:2004 Electrical Fast Transient/Burst (EFT) 1 kV on data cables EN61000-4-6:2009 Conducted immunity requirements, 3 Vrms on data cables 150 kHz to 80 MHz
RoHS (EU Directive 2002/95/EG)	Compliant (as of July 1st, 2006)