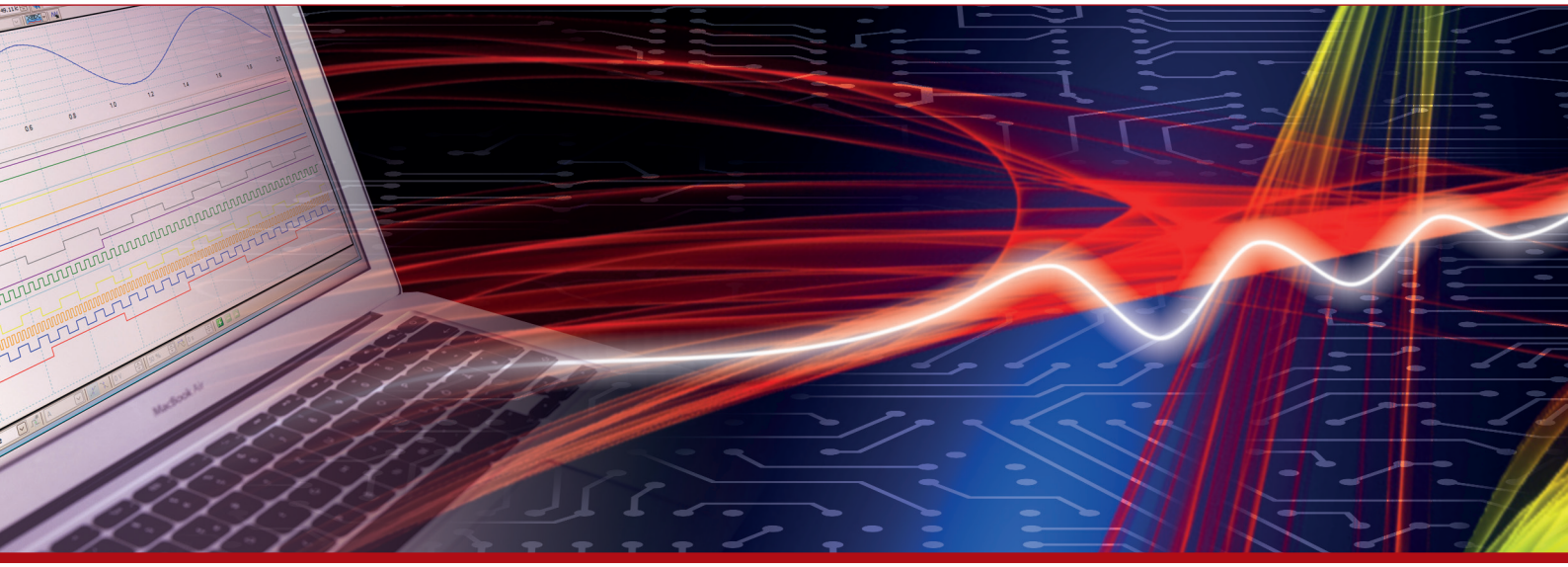
Product Datasheet - Technical Specifications



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1480A Overview

- Organizes the USB protocol data into an hierarchical tree view which reflects the nesting of the actual USB protocol on the bus.
- Supports all USB 2.0 speeds (Low-speed, Full-speed and High-speed)
- Automatically detects link speed as USB devices are connected to the link under test
- FPGA-based design allows automatic update of firmware and software without user involvement
- Decodes and displays all standard USB Descriptors, Transactions and Packets for easy and quick analysis
- Decodes and displays all bus events down to the most detailed differential D-/D+ bus state changes with 16.67 ns resolution.
- Drivers and software are available for all 32-bit and 64-bit Windows platform (Windows XP and newer)
- A very small physical format and a bus-powered design allows easy transportation and convenient use with laptops (only 4.90" x 4.10" x 1.4" / 8.8oz or 125 x 105 x 35 mm / 250g).
- Designed, manufactured and supported in the U.S.A.

International Test Instruments Corporation

ITIC 1480A USB 2.0 Protocol Analyzer

International Test Instruments Corporation

Quality Engineering—Quality Instruments

1480A Software Overview

The 1480A software decodes and displays the captured USB data in a hierarchical tree view which allows large amounts of data to be displayed in very compact form.

USB Descriptors, Transactions and Packets are decoded in great detail which allows easy bus traffic analysis at a mere glance.

USB devices communicated with during the capture session are displayed in a separate 'Discovered Devices' view which enables device enumerations to be found quickly in the trace data.

The 'Node Finder' view records statistics about captured packets and transactions and allows direct jumps to any information in the trace, even if located deep inside the protocol hierarchy.

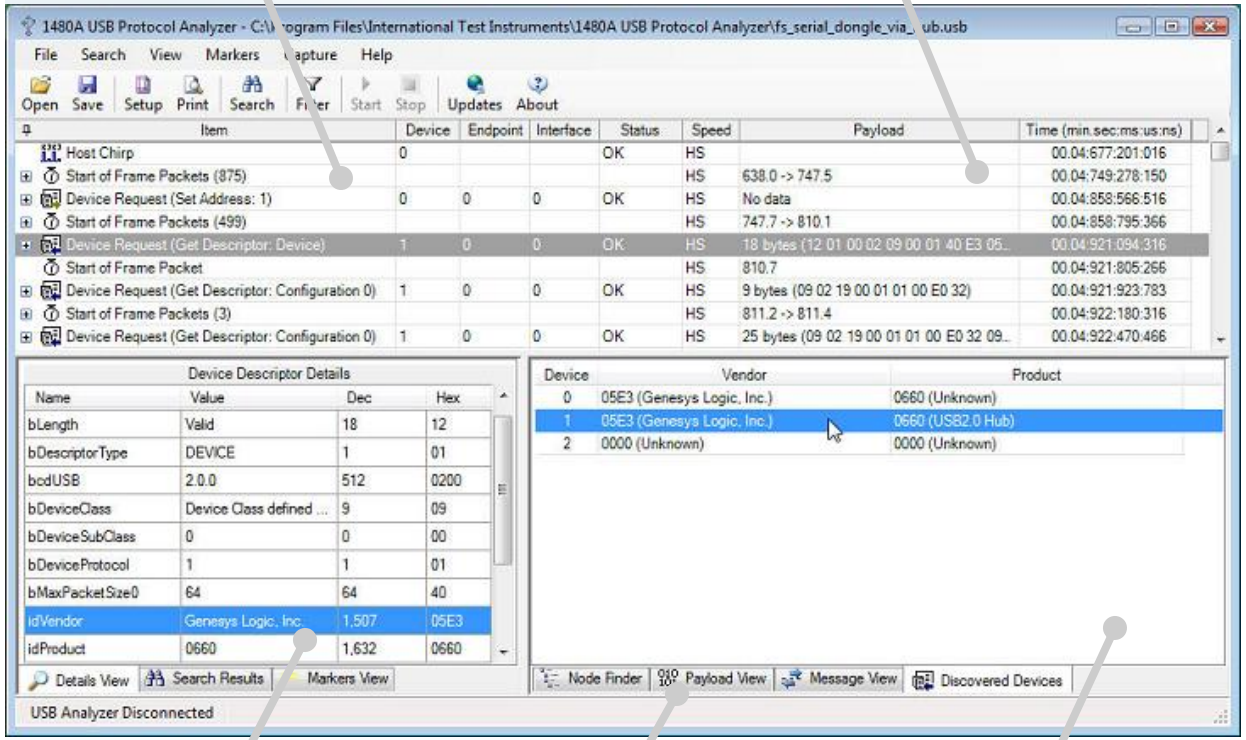
Visit our web site for a complete 1480A software tutorial and software downloads.

Hierarchical Protocol Tree View

Organizes the USB protocol data into an hierarchical tree view which reflects the nesting of the actual USB protocol on the bus. This greatly eases understanding of the USB protocol.

USB Protocol Item Data

The right side of the Protocol View displays payload data for the selected protocol item as well as relative or absolute timestamps with 16.67 ns resolution.



Details View

Displays the details of the selected Device Request, Transaction or Packet. Additional tabs also display search results and trace marker views.

Additional Views

Various views are available that ease navigation to any protocol item, display of hexadecimal payload data and display of low-level PHY data.

Discovered Devices View

Displays and allows quick navigation to the connection sequence of all discovered devices in the trace data.

Model 1480A
USB 2.0 Protocol Analyzer

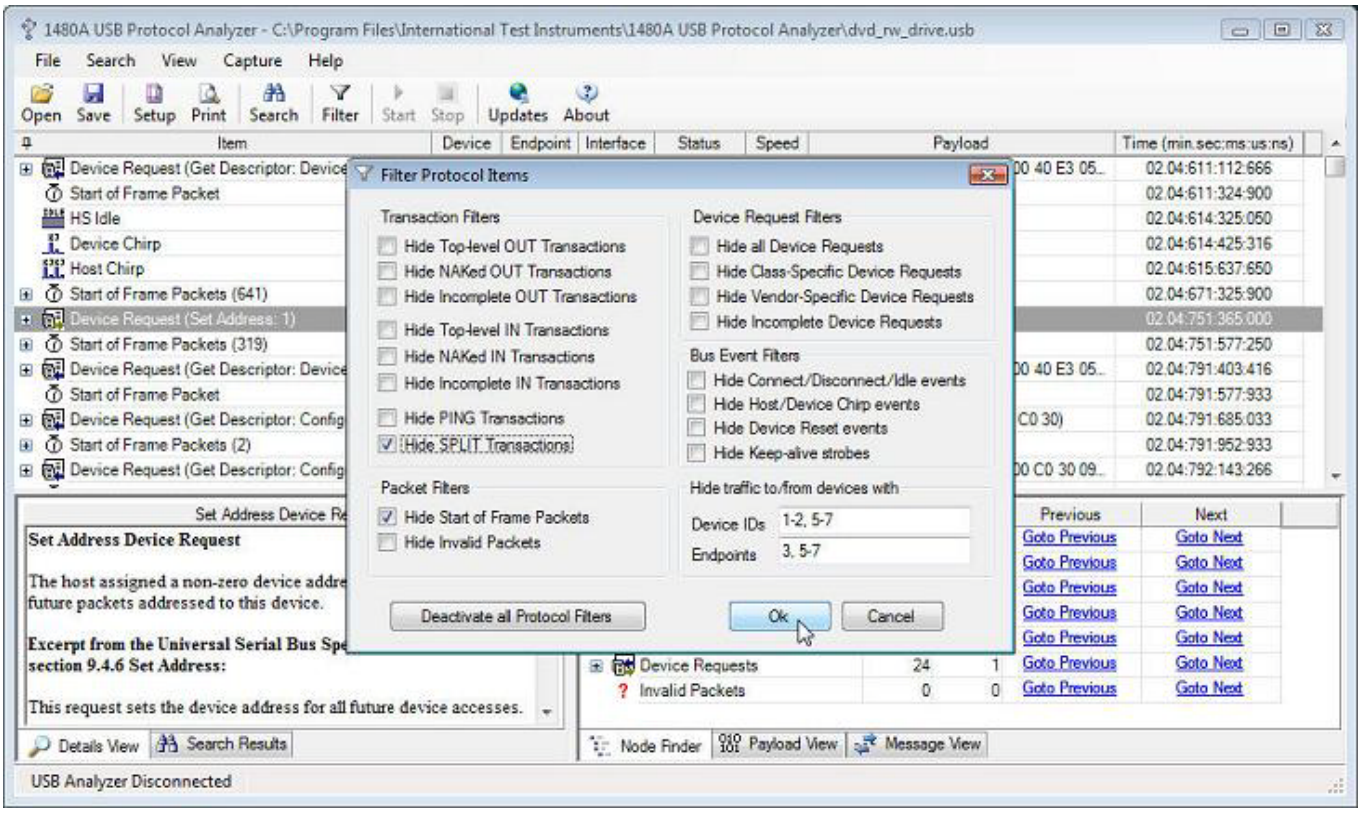
Description

The Model 1480A USB 2.0 Protocol Analyzer with OTG decoding is specifically designed for the road-warrior. It will easily slip into your coat pocket or laptop bag for those trips where bringing a large USB analyzer is not convenient. The physical format is very small, only slightly larger than a pen or a computer mouse. The enclosure is made out of very high-quality brushed aluminum.

The data captured is in real-time transferred to the Analysis PC where it is analyzed and displayed by the PC Software. The USB Analyzer has no limitation of the data size captured as data is streamed in real-time directly from the link under test into the PC application's tree view display. This allows you to capture many hundreds of MB of data (only limited to the size of RAM in your analysis PC).

The 1480A contains a 32MB FIFO buffer SDRAM that smooths out bursty traffic such that temporarily bursty traffic on the link under test will not cause the USB Analyzer-to-Analysis PC link to be saturated. The sustained maximum capture speed to the analysis PC largely depends on the speed of the capture PC. As a rule of thumb, as long as the throughput on the link under test is under 15 MB / s then the analysis PC will keep up with the captured data speed without the buffer FIFO filling up. Note that the 1480A USB Analyzer will never lose captured data (regardless if the link under test is saturated) since the captured data is always buffered in the SDRAM FIFO before being sent to the analysis PC.

The 1480A USB Protocol Analyzer is FPGA-based which makes it fully programmable with each new software upgrade. This allows us to fully remotely deploy logic and software upgrades, if needed. This means that you will never need to send your hardware to us for upgrade as more advanced software like class decoders are purchased.



The PC Analysis Software displays data as it is received from the USB Analyzer hardware so you will not have to wait for lengthy data decoding before you can start analyzing the captured data. As USB Transactions and Packets are captured, they will be decoded and added to the tree view in the PC Analysis software. This makes it very easy to understand the sequence of events in the captured data. Detail views display the details for selected Transactions and Packets in the tree view as they are clicked on. The PC Analysis software also decodes payload data in hex format and displays it in the hex view pane.

To learn more about the PC Analysis Software, click here. The USB analysis software is free. It includes sample LS, FS and HS data files that can be viewed in the software, enabling you to get familiar with the Software before buying the USB Analyzer hardware.

What's in the box?

- 1480A USB 2.0 Protocol Analyzer.
- Two 3ft (1m) USB 2.0 cables.
- Installation CD containing drivers and software.

Technical Specifications

1480A LS/FS/HS USB Protocol Analyzer Technical Specifications.	
Dimensions / Weight	4.90” x 4.10” x 1.4” / 8.8oz (125 x 105 x 35 mm / 250g)
Analysis PC Requirements	32-bit (x86) and 64-bit (x64) Windows versions (XP SP2 or newer). Pentium 4 or faster CPU is recommended.
Supported USB Standards	USB 1.0, USB 1.1, USB 2.0, OTG 1.3.
Supported USB Speeds	The 1480A automatically detects device connection in high speed (480 Mbps), full speed (12 Mbps), and low speed (1.5 Mbps). Note: HS Devices are initially connected as FS devices. Only after successfully having completed the Device and Host Chirp Sequences do HS-capable devices enter HS mode. The 1480A fully supports automatic detection of both Device and Host Chirp.
Maximum recorded data length	Unlimited. Only the available disk and memory of the Analysis PC limits how much data can be captured and analyzed.
Built in FIFO buffer	32 MB. The FIFO buffer is used to smooth out the data stream captured from the Link Under Test. Note that the FIFO buffer will fill up if the Analysis PC is unable to read out data fast enough from the 1480A. In this case, the recording will automatically stop and the PC application will display the captured data up until the point where the FIFO filled up.
Analysis PC Interface	USB 2.0 Type "B" Connector
Link Under Test Interface	USB 2.0 Type "A" and "B" Connectors.
LED Indicators	• Host Power: Indicates when the 1480A unit is powered and the Analysis PC Device Drivers have been installed. • Link Power: Indicates that the Link Under Test is powered by the Host. • Link Activity: Indicates when link activity is detected.

Captured bus events and packets	All bus activity down to the smallest detail is captured and stored into the .usb file when recording. The 1480A Software displays all the captured information from the lowest link level up to the highest protocol level. In addition the VBus voltage is continuously monitored and stored in the capture file. For detailed information of the captured data, please see the datasheet for the NXP ISP1505A USB Transceiver.
Displayed Bus Events	LS Device Connection, FS Device Connection, HS Device Connection, Device Reset, Device Chirp, Host Chirp, Device Disconnection, HS Idle, Keep-Alives, OTG Session Request Protocol, OTG Host Negotiation Protocol and OTG VBus events.
Displayed Packets.	SETUP, IN, OUT, SOF, DATA0, DATA1, DATA2, MDATA, ACK, NAK, NYET, STALL, PING, SPLIT, PRE.
Displayed Transactions.	SETUP Transaction, IN Transaction, OUT Transaction, PING Transactions, SPLIT Transactions.
Decoded Device Requests	CLEAR_FEATURE, SET_FEATURE, SET_ADDRESS, GET_DESCRIPTOR, SET_DESCRIPTOR, GET_STATUS, GET_CONFIGURATION, SET_CONFIGURATION, GET_INTERFACE, SET_INTERFACE, SYNCH_FRAME. Note: All Device Requests are captured and displayed but only standard Device Requests are decoded. I.e., non-standard Device Requests (not listed above) will be displayed in hexadecimal form.
Decoded Descriptors	Device Descriptor, Configuration Descriptor, Interface Descriptor, Endpoint Descriptor, String Descriptor, Device_Qualifier Descriptor, Other_Speed_Configuration Descriptor and OTG Descriptor. Note: Class-specific descriptors are currently not decoded but instead displayed in hexadecimal form. Class Decoders, sold separately when available, will fully decode related class-specific descriptors.
Packet Integrity Checked	• Token Packets: PID and CRC-5 errors are flagged as invalid. • Data Packets: CRC-16 errors are flagged as invalid.