RedLab 1408FS-Plus

Analog and Digital I/O

User's Guide

MEILHAUS
ELECTRONIC

Table of Contents

About this User's Guide

What you will learn from this user's guide

This user's guide describes the Meilhaus Electronic RedLab 1408FS-Plus data acquisition device and lists device specifications.

Conventions in this user's guide

For more information
Text presented in a box signifies additional information and helpful hints related to the subject matter.

Caution! Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

bold text   **Bold** text is used for the names of objects on a screen, such as buttons, text boxes, and check boxes.

italic text   *Italic* text is used for the names of manuals and help topic titles, and to emphasize a word or phrase.

Where to find more information

Additional information about RedLab 1208FS-Plus hardware is available on our website at www.meilhaus.com. You can also contact Meilhaus Electronic GmbHwith specific questions.

- Phone: +49 (0) 81 41/52 71-0
- Fax: +49 (0) 81 41/52 71-129
- E-Mail: support@meilhaus.com

Introducing the RedLab 1408FS-Plus

The RedLab 1408FS-Plus is an analog input and digital I/O data acquisition device that provides the following features:

- Eight analog input channels that are software configurable for either eight 13-bit single-ended inputs or four 14-bit differential inputs
- Two 12-bit analog output channels
- 16 digital I/O channels that are independently-selectable as input or output in two 8-bit ports
- 32-bit event counter input for counting TTL pulses
- External digital trigger input
- Bidirectional terminal for external clocking or multi-unit synchronization
- Screw terminals for field wiring connections

The device is powered by the +5 V USB supply from the computer. No external power is required.

The RedLab 1408FS-Plus is compatible with both USB 1.1 and USB 2.0 ports. The speed of the device may be limited when using a USB 1.1 port due to the difference in transfer rates on the USB 1.1 versions of the protocol (low-speed and full-speed).

Functional block diagram

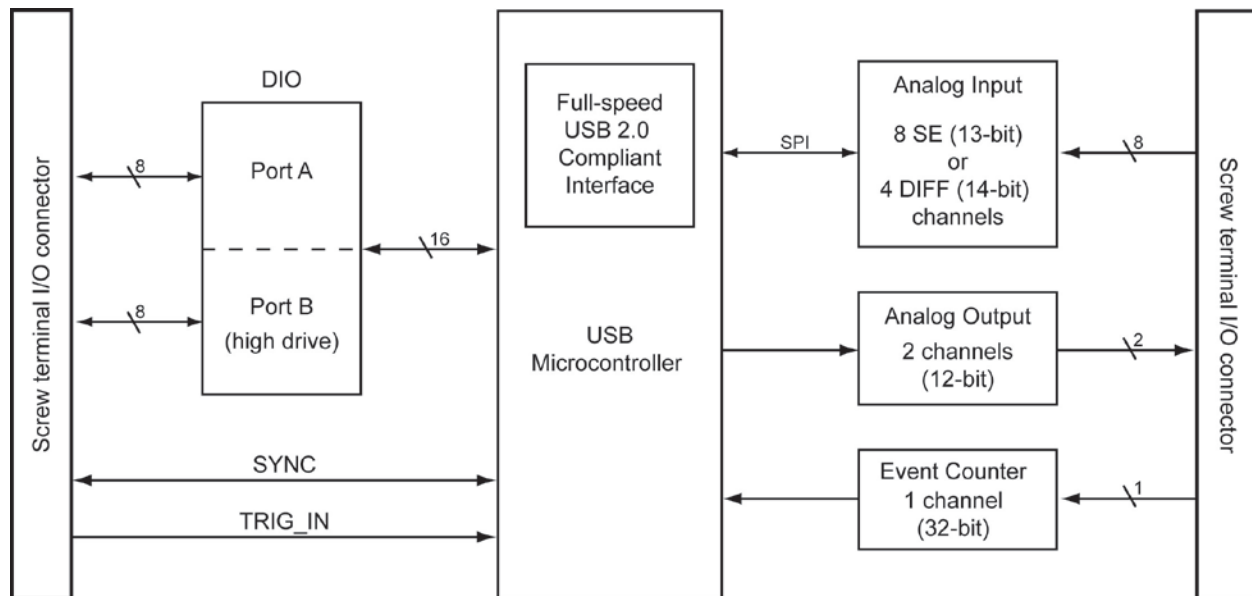Device functions are illustrated in the block diagram shown here.

Figure 1. RedLab 1408FS-Plus functional block diagram

Installing the RedLab 1408FS-Plus

What comes with your shipment?

Verify that the following hardware components are included in the shipment.

Hardware

- RedLab 1408FS-Plus
- USB cable

Software

Documentation

Unpacking

As with any electronic device, you should take care while handling to avoid damage from static electricity. Before removing the RedLab 1408FS-Plus from its packaging, ground yourself using a wrist strap or by simply touching the computer chassis or other grounded object to eliminate any stored static charge.

If any components are missing or damaged, contact us immediately using one of the following methods:

Additional information about RedLab 1208FS-Plus hardware is available on our website at www.meilhaus.com. You can also contact Meilhaus Electronic GmbH with specific questions.

- Phone: +49 (0) 81 41/52 71-0
- Fax: +49 (0) 81 41/52 71-129
- E-Mail: support@meilhaus.com

Installing the software

Universal Library and InstaCal

Install Universal Library and InstaCal when you want to develop data acquisition applications using Windows programming languages.

Universal Library and InstaCal software are included on the CD that ships with the device. Refer to the *Quick Start Guide* booklet for instructions about installing Universal Library and InstaCal software.

Installing the hardware

> **Install the software before you install your device**
>
> The driver needed to run the device is installed when you install the software. Therefore, you need to install the software package you plan to use before you install the hardware.
>
> For operation on a Windows operating system, we recommend that you run Windows Update to update your operating system with the latest USB drivers.

To connect the device to your system, turn on your computer and connect the USB cable to an available USB port on the computer or to an externally powered USB hub connected to the computer. Connect the other end of the USB cable to the USB connector on the device. No external power is required.

When connected for the first time, a **Found New Hardware** dialog opens when the operating system detects the device. When the dialog box closes, the installation is complete. The LED turns on after the device is successfully installed.

Caution! Do not disconnect any device from the USB bus while the computer is communicating with the device, or you may lose data and/or your ability to communicate with the device.

If the LED turns off

If the LED is on but then turns off, the computer has lost communication with the device. To restore communication, disconnect the USB cable from the computer and then reconnect it. This should restore communication, and the LED should turn on.

Calibrating the hardware

The Meilhaus Electronic Manufacturing Test department performs the initial factory calibration. Return the device to Meilhaus Electronic GmbHwhen calibration is required. The recommended calibration interval is one year.

The RedLab 1408FS-Plus does not support field calibration.

Functional Details

Analog input acquisition modes

The RedLab 1408FS-Plus can acquire analog input data in either software paced or continuous scan mode.

Software paced

The RedLab 1408FS-Plus acquires data one analog sample at a time using software-paced mode. You initiate the A/D conversion by calling a software command. The analog value is converted to digital and returned to the computer. You can repeat this procedure until you have the total number of samples that you want.

The RedLab 1408FS-Plus can attain throughput sample rate in software paced mode is system-dependent.

Hardware paced

The RedLab 1408FS-Plus can acquire data from up to eight channels using hardware-paced mode. The analog data is acquired and converted to digital values until you stop the scan. Data is transferred in blocks of 32 samples minimum from the device to the memory buffer on your computer.

The A/D converter is paced by either an internal or external clock source.

The maximum scan rate is an aggregate rate. The total sample rate for all channels cannot exceed 48 kS/s. The following table lists the sample rate when scanning from one to eight channels.

Maximum per channel sample rate

# channels scanned	Sample rate (kS/s)
1	48
2	24
3	16
4	12
5	9.60
6	8
7	6.85
8	6

You can start a hardware-paced scan with a software command. Optionally, hardware-paced scans can be delayed by an external hardware trigger event.

External components

The external components – screw terminal banks, LED, and USB connector –are shown in Figure 2.

1	Screw terminal pins 21 to 40	3	Screw terminal pins 1 to 20
2	LED	4	USB connector

Figure 2. External components

USB connector

Receives the supplied USB cable. When connected to a computer or USB hub, the cable provides +5 V power and communication. No external power supply is required.

LED

The following table lists the behavior of the device LED.

LED state	Indication
Steady green	The device is connected to a computer or external USB hub.
Blinks continuously	Data is being transferred.

Screw terminals

The screw terminals provide the following connections:

- Eight analog input connections (**CH0 IN** to **CH7 IN**, **CH0 IN HI/LO** through **CH3 IN HI/LO**)
- Two analog output connections (**D/A OUT 0** to **D/A OUT 1**)
- 16 digital I/O connections (**PortA0** to **Port A7**, and **Port B0** to **Port B7**)
- External trigger input (**TRIG_IN**)
- External counter input (**CTR**)
- Bidirectional terminal for external clocking or multi-unit synchronization (**SYNC**)
- Power output (**+VO**)
- Analog ground (**AGND**) and ground (**GND**)

Use 16 AWG to 30 AWG wire when making connections to the screw terminals.
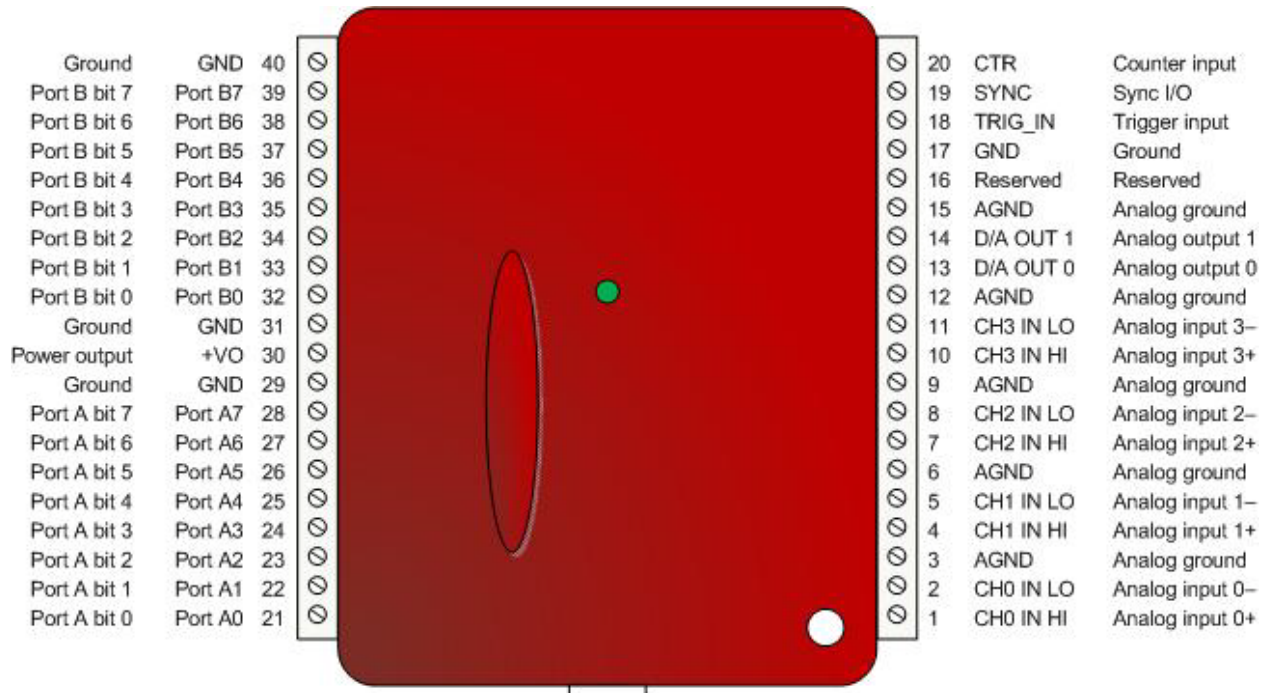
The single-ended mode pinout is shown in Figure 3.

Ground	GND	40				20	CTR	Counter input
Port B bit 7	Port B7	39				19	SYNC	Sync I/O
Port B bit 6	Port B6	38				18	TRIG_IN	Trigger input
Port B bit 5	Port B5	37				17	GND	Ground
Port B bit 4	Port B4	36				16	Reserved	Reserved
Port B bit 3	Port B3	35				15	AGND	Analog ground
Port B bit 2	Port B2	34				14	D/A OUT 1	Analog output 1
Port B bit 1	Port B1	33				13	D/A OUT 0	Analog output 0
Port B bit 0	Port B0	32				12	AGND	Analog ground
Ground	GND	31				11	CH3 IN LO	Analog input 3–
Power output	+VO	30				10	CH3 IN HI	Analog input 3+
Ground	GND	29				9	AGND	Analog ground
Port A bit 7	Port A7	28				8	CH2 IN LO	Analog input 2–
Port A bit 6	Port A6	27				7	CH2 IN HI	Analog input 2+
Port A bit 5	Port A5	26				6	AGND	Analog ground
Port A bit 4	Port A4	25				5	CH1 IN LO	Analog input 1–
Port A bit 3	Port A3	24				4	CH1 IN HI	Analog input 1+
Port A bit 2	Port A2	23				3	AGND	Analog ground
Port A bit 1	Port A1	22				2	CH0 IN LO	Analog input 0–
Port A bit 0	Port A0	21				1	CH0 IN HI	Analog input 0+

Figure 3. Single-ended mode pinout

The differential mode pinout is shown in Figure 4.

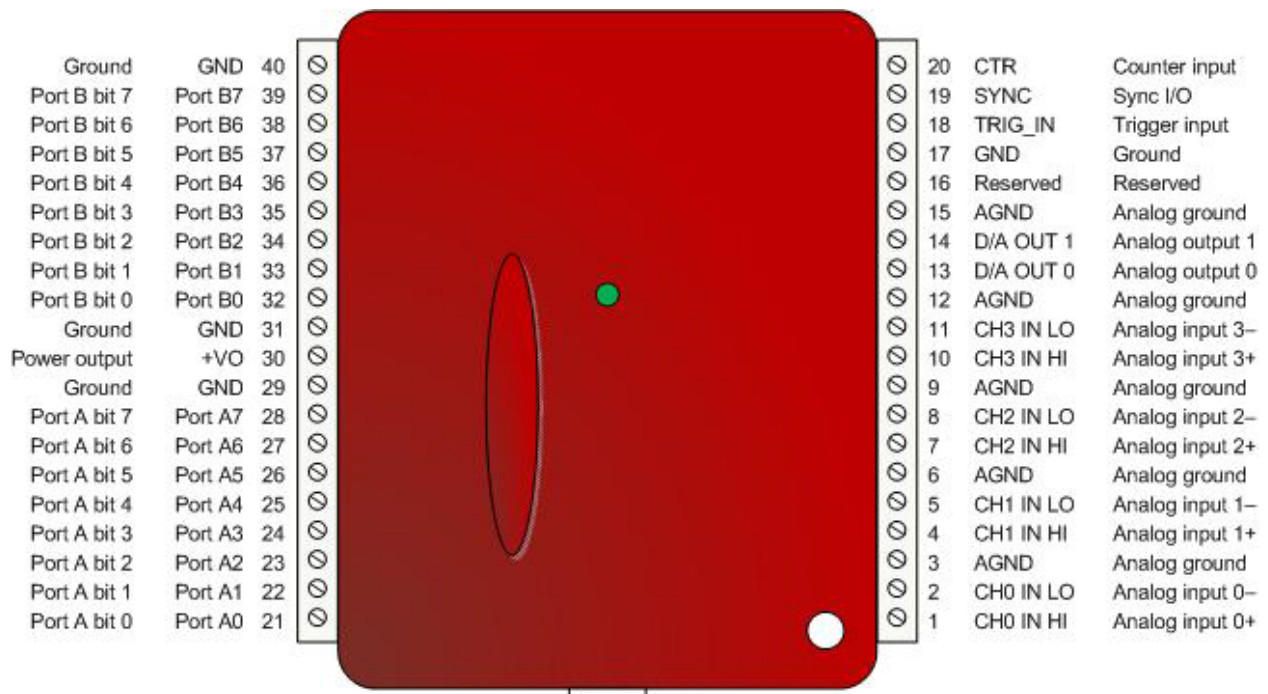| Ground	GND	40				20	CTR	Counter input
Port B bit 7	Port B7	39				19	SYNC	Sync I/O
Port B bit 6	Port B6	38				18	TRIG_IN	Trigger input
Port B bit 5	Port B5	37				17	GND	Ground
Port B bit 4	Port B4	36				16	Reserved	Reserved
Port B bit 3	Port B3	35				15	AGND	Analog ground
Port B bit 2	Port B2	34				14	D/A OUT 1	Analog output 1
Port B bit 1	Port B1	33				13	D/A OUT 0	Analog output 0
Port B bit 0	Port B0	32				12	AGND	Analog ground
Ground	GND	31				11	CH3 IN LO	Analog input 3–
Power output	+VO	30				10	CH3 IN HI	Analog input 3+
Ground	GND	29				9	AGND	Analog ground
Port A bit 7	Port A7	28				8	CH2 IN LO	Analog input 2–
Port A bit 6	Port A6	27				7	CH2 IN HI	Analog input 2+
Port A bit 5	Port A5	26				6	AGND	Analog ground
Port A bit 4	Port A4	25				5	CH1 IN LO	Analog input 1–
Port A bit 3	Port A3	24				4	CH1 IN HI	Analog input 1+
Port A bit 2	Port A2	23				3	AGND	Analog ground
Port A bit 1	Port A1	22				2	CH0 IN LO	Analog input 0–
Port A bit 0	Port A0	21				1	CH0 IN HI	Analog input 0+

Figure 4. Differential mode pinout

Signal connections

Analog input

You can connect up to eight analog input connections to the screw terminal containing pins 1 to 20 (**CH0 IN** through **CH7 IN**.)

You can configure the analog input channels as eight single-ended channels or four differential channels. When configured for differential mode, each analog input has 14-bit resolution. When configured for single-ended mode, each analog input has 13-bit resolution, due to restrictions imposed by the A/D converter.

Single-ended configuration

When configured for single-ended input mode, the input signal is referenced to signal ground (GND) and delivered through two wires:

- Connect the wire carrying the signal to be measured to **CH# IN**.
- Connect the second wire to **AGND**.

The input range for single-ended mode is ±10 V. The single-ended mode pinout is shown in Figure 3 Seite 10.

Differential configuration

When configured for differential input mode, the input signal is measured with respect to the low input and delivered through three wires:

- Connect the wire carrying the signal to be measured to **CH# IN HI**
- Connect the wire carrying the reference signal to **CH# IN LO**
- Connect the third wire to **GND**.

The differential mode pinout is shown in Figure 4 Seite 10.

Note: To perform a single-ended measurement using differential channels, connect the signal to **CH# IN HI** and ground the associated **CH# IN LO** input.

A low-noise precision programmable gain amplifier (PGA) is available on differential channels to provide gains of up to 20 and a dynamic range of up to 14-bits. Differential mode input voltage ranges are ±20 V, ±10 V, ±5 V, ±4 V, ±2.5 V, ±2.0 V, ±1.25 V, and ±1.0 V.

In differential mode, the following two requirements must be met for linear operation:

- Any analog input must remain in the −10V to +20V range with respect to ground at all times.
- The maximum differential voltage on any given analog input pair must remain within the selected voltage range.

The input [*common-mode voltage + signal*] of the differential channel must be in the −10 V to +20 V range in order to yield a useful result.

For example, you input a 4 V pp sine wave to CH# IN HI, and apply the same sine wave 180° out of phase to CH# IN LO. The common mode voltage is 0 V. The differential input voltage swings from 4 V – (–4 V) = 8 V to –4 V – (4 V) = –8V. Both inputs satisfy the –10 V to +20 V input range requirement, and the differential voltage is suited for the ±10 V input range (see Figure 5).
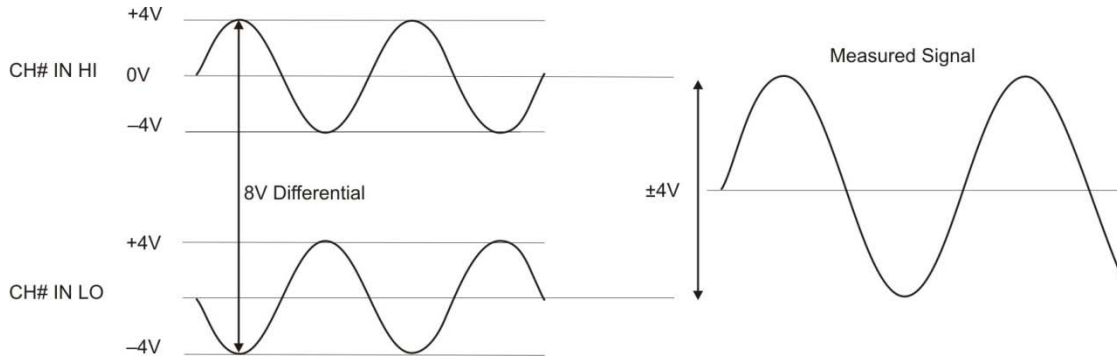
Figure 5. Differential voltage example: common mode voltage of 0 V

If you increase the common mode voltage to 11 V, the differential remains at ±8 V. Although the [*common-mode voltage + signal*] on each input now has a range of +7 V to +15 V, both inputs still satisfy the –10 V to +20 V input requirement (see Figure 6).
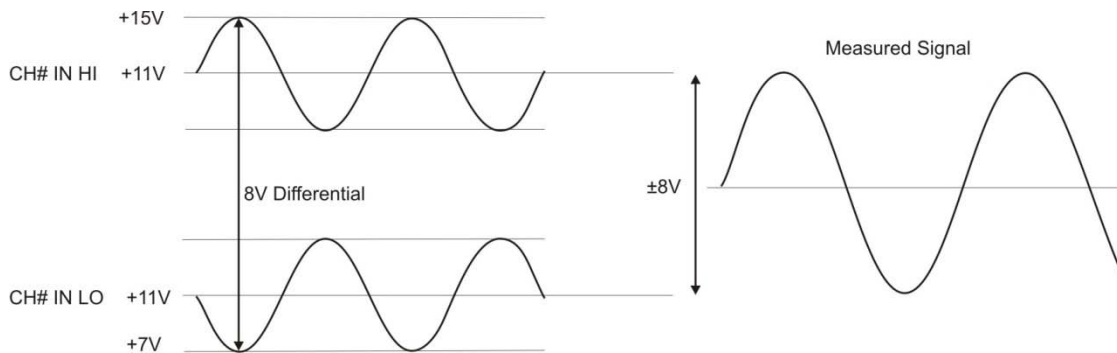

Figure 6. Differential voltage example: common mode voltage of 11 V

If you decrease the common-mode voltage to –7 V, the differential stays at ±8 V. However, the solution now violates the input range condition of –10 V to +20 V. The voltage on each analog input now swings from –3 V to –11 V. Voltages between –10 V and –3 V are resolved, but those below –10 V are clipped, as shown in Figure 7.
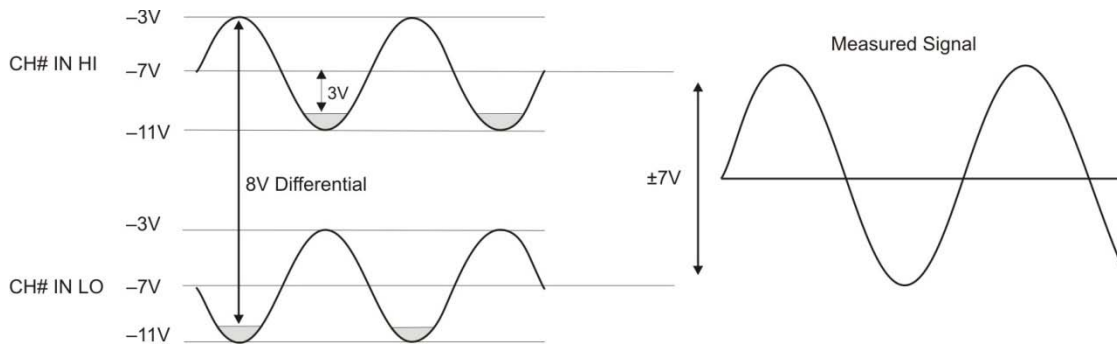

Figure 7. Differential voltage example: common mode voltage of –7 V

Since the analog inputs are restricted to a −10 V to +20 V signal swing with respect to ground, all ranges *except* ±20V can realize a linear output for any differential signal with zero common mode voltage and full scale signal inputs. The ±20 V range is the exception. You cannot put −20 V on CH# IN HI and 0 V on CH# IN LO, since this violates the input range criteria.

The table below shows some possible inputs and the expected results.

Sample inputs and differential results

CH# IN HI	CH# IN LO	Result
−20 V	0 V	Invalid

−15 V	+5 V	Invalid
−10 V	0 V	−10 V
−10 V	+10 V	−20 V
0 V	+10 V	−10 V
0 V	+20 V	−20 V
+10 V	−10 V	+20 V
+10 V	0 V	+10 V
+15 V	−5 V	+20 V
+20 V	0	+20 V

Channel-Gain queue

The channel gain queue feature allows you to set up a scan sequence with a unique per-channel gain setting and channel sequence. The settings are stored in a channel-gain queue list that is written to local memory on the device. The gain queue can contain up to eight elements in single-ended mode, and up to four elements in differential mode.

The elements must be unique and listed in ascending order. An example of a four-element list is shown in the table below.

Sample channel-gain queue list

Element	Channel	Range	Gain
0	CH0	BIP20V	1
1	CH1	BIP5V	4
2	CH2	BIP10V	2
3	CH3	BIP2V	10

When a scan begins with the gain queue enabled, the device reads the first element, sets the appropriate channel number, range, and gain, and then acquires a sample. The properties of the next element are then retrieved, and another sample is acquired. This sequence continues until all elements in the gain queue have been selected.

When the end of the channel list is detected, the sequence returns to the first element in the list. The sequence repeats until the specified number of samples is acquired.

Carefully match the gain to the expected voltage range on the associated channel or an over range condition may occur. Although this condition does not damage the device, it does produce a useless full-scale reading, and can introduce a long recovery time due to saturation of the input channel.

Analog output

You can connect up to two analog output connections to **D/A OUT 0** and **D/A OUT 1**. Each channel can be paced at rates up to 50,000 updates per second. The output range is 0 V to 5 V.

Digital I/O

The device has 16 DIO channels that are configured as two 8-bit ports – Port A and Port B. Port B is high drive. You can connect up to eight DIO lines to **Port A0** to **Port A7** and up to eight DIO lines to **Port B0** to **Port B7**. You can configure each port for either input or output. The digital ports are set for input when the device is powered on or reset.

When configured for input, the digital I/O terminals can detect the state of any TTL-level. Refer to the schematic shown in Figure 8.
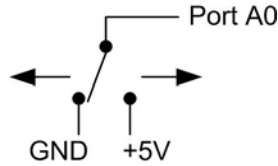
Figure 8. Schematic showing switch detection by digital channel Port A0

If you set the switch to the +5 V input, Port A0 reads *TRUE* (1). When set to GND, Port A0 reads *FALSE* (0).

Pull-up/down configuration

All digital I/O lines are pulled high to USB +5 V with a 47 kΩ resistor by default. You can change the pull-up/down configuration using internal jumpers. You must remove the device housing to access the jumpers on the circuit board.

Complete the following steps to set the jumper for pull-up or pull-down:

1. Unplug the device from the computer.

2. Turn the device over and rest the top of the housing on a flat, stable surface.

Caution! The discharge of static electricity can damage some electronic components. Before removing the RedLab 1408FS-Plus from its housing, ground yourself using a wrist strap or touch the computer chassis or other grounded object to eliminate any stored static charge.

3. Remove the three screws from the bottom of the device using a #1 Philips head screwdriver.

4. Hold both the top and bottom sections together, turn the device over and rest it on the surface, then carefully remove the top section of the case to expose the circuit board.

    The user-configurable jumpers are labeled **DIO A** and **DIO B**. Figure 9 shows the location of each jumper on the circuit board.
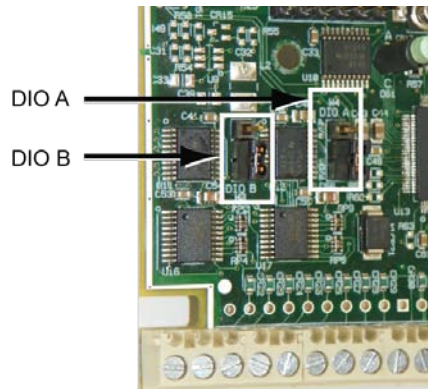

Figure 9. Pull-up/down jumper locations

5. Set each jumper for pull-up or pull-down, as shown in Figure 10. Use the jumper labeled **DIO A** to configure Port A, and **DIO B** to configure Port B.
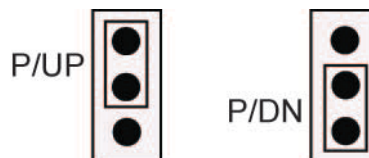

Figure 10. Pull-up/down jumper configuration

6. Replace the top section of the housing, and fasten it to the bottom section with the three screws.

For more information on digital signal connections

For more information on digital signal connections and digital I/O techniques, refer to the *Guide to Signal Connections* (available on our web site at www.mccdaq.com/signals/signals.pdf).

Counter input

The **CTR** terminal is a 32-bit event counter that can accept frequency inputs up to 1 MHz. The internal counter increments when the TTL levels transition from low to high.

Trigger input

The **TRIG_IN** connection is an external trigger input that you can configure for either rising or falling edge.

SYNC I/O

The **SYNC** terminal is a bidirectional I/O signal that can be configured as an input (default) or an output.

- Configure as an external clock input to pace the A/D conversions from an external source. The SYNC terminal supports TTL-level input signals of up to 48 kHz.
- Configure as an output to pace the conversions on a second device and acquire data from 16 channels using one clock. For more information about synchronized operations see page 18.

Power output

The **+VO** connection draws power from the USB connector on the computer.

Caution! The +VO terminal is an output. Do not connect to an external power supply or you may damage the RedLab 1408FS-Plus and possibly the computer.

Ground

The analog ground (**AGND**) terminals provide a common ground for all analog channels.

The digital ground (**GND**) terminals provide a common ground for the digital, trigger, counter, and sync channels and the power terminal.

Accuracy

The overall accuracy of any instrument is limited by the error components within the system. Resolution is often incorrectly used to quantify the performance of a measurement product. While "14-bits" or "1 part in 16384" does indicate what can be resolved, it provides little insight into the quality of an absolute measurement. Accuracy specifications describe the actual results that can be realized with a RedLab 1408FS-Plus.

There are three types of errors which affect the accuracy of a measurement system:

- offset
- gain
- nonlinearity

The primary error sources in the RedLab 1408FS-Plus are offset and gain. Nonlinearity is small in each device, and is not significant as an error source with respect to offset and gain.

Figure 11 shows an ideal, error-free transfer function. The typical calibrated accuracy is range-dependent. Refer to the "Accuracy specifications" Seite 21 for more information. We use a ±10 V range here as an example of what you can expect when performing a measurement in this range.
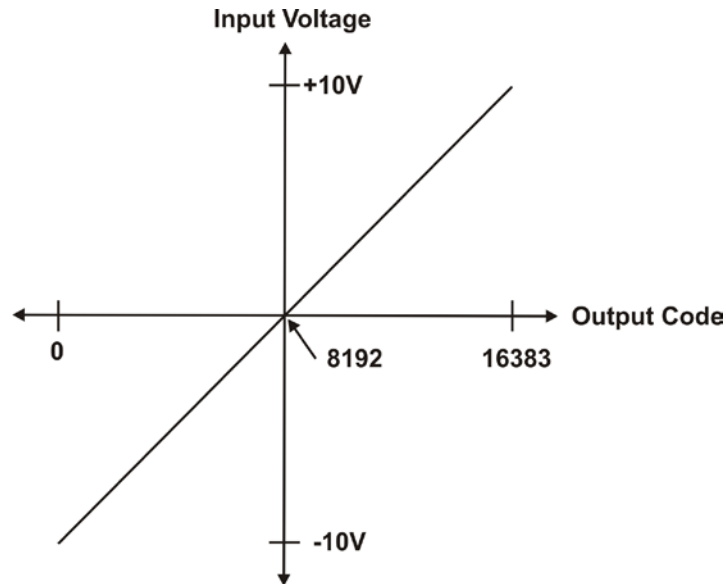

Figure 11. Ideal ADC transfer function

Figure 12 shows an example of a transfer function with a ±2.44 mV offset error. Offset error affects all codes equally by shifting the entire transfer function up or down along the input voltage axis.

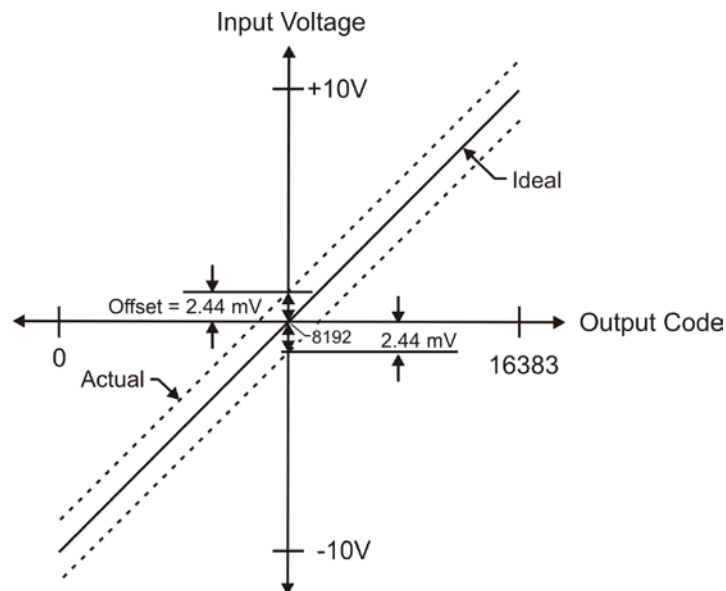The accuracy plots in Figure 12 are drawn for clarity and are not drawn to scale.

Figure 12. ADC transfer function with offset error

Gain error is a change in the slope of the transfer function from the ideal, and is typically expressed as a percentage of full-scale. Figure 13 shows the transfer function with gain error. Gain error is easily converted to voltage by multiplying the full-scale (**FS**) input by the error.

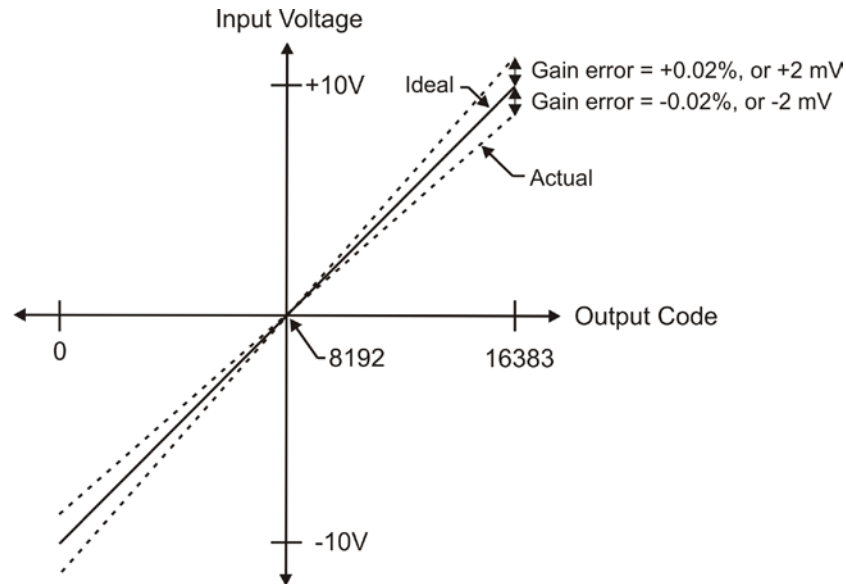The accuracy plots in Figure 13 are drawn for clarity and are not drawn to scale.

Figure 13. ADC Transfer function with gain error

Figure 14 shows an example of a transfer function with a calibrated gain error of ±0.02%, or ±2 mV. This means that at full scale, neglecting the effect of offset for the moment, the measurement would be within 2 mV of the actual value. Note that gain error is expressed as a ratio. Values near ±FS are more affected from an absolute voltage standpoint than are values near mid-scale, which see little or no voltage error.

Combining these two error sources in Figure 14, we have a plot of the error band of the ±10 V range. This is a graphical version of the typical accuracy specification of the product.

The accuracy plots in Figure 14 are drawn for clarity and are not drawn to scale.
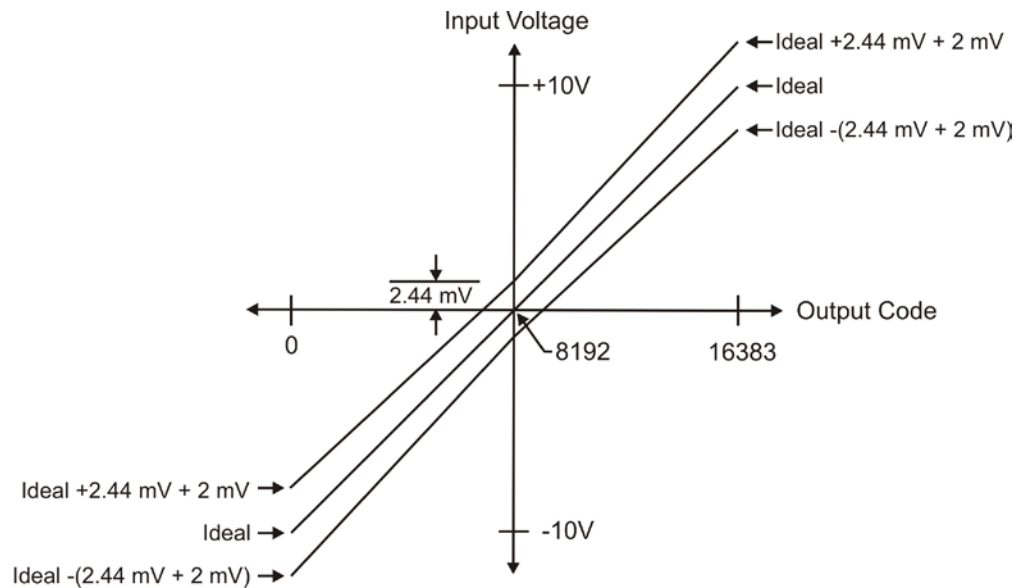
Figure 14. Error band plot

Synchronized operations

You can connect the SYNC pin of two devices together in a master/slave configuration and acquire data from the analog inputs of both devices using one clock.

When the SYNC pin is configured as an output, the internal A/D pacer clock signal is sent to the screw terminal. Output the clock signal to the SYNC pin of a second device that is configured for A/D pacer input.

Power

Connecting the device to a computer draws <100 mA of current from the USB +5V supply. When running applications, the current that can be drawn from all device connections (analog, digital, SYNC, and +VO output loading) is <500 mA. The maximum output current that is available at the +VO power output terminal is 100 mA.

With all outputs at their maximum output current, the RedLab 1408FS-Plus in a fully-loaded configuration may be above that allowed by the computer. In this case, determine the per-pin loading in the application to ensure that the maximum loading criteria is met. The per-pin loading is calculated by dividing +5V by the load impedance of the pin in question.
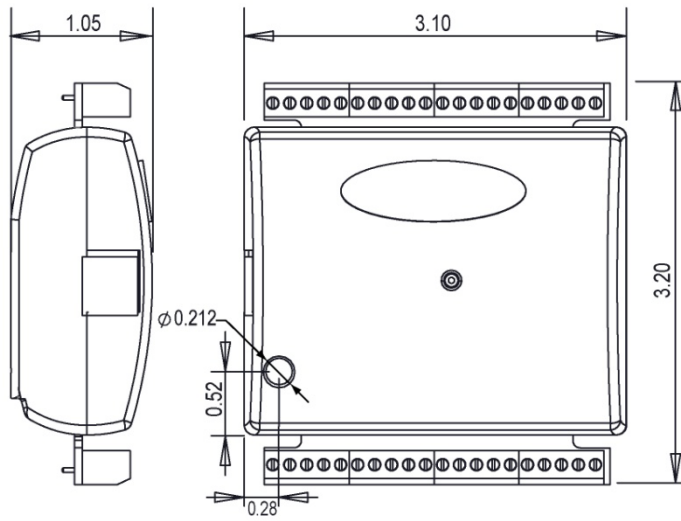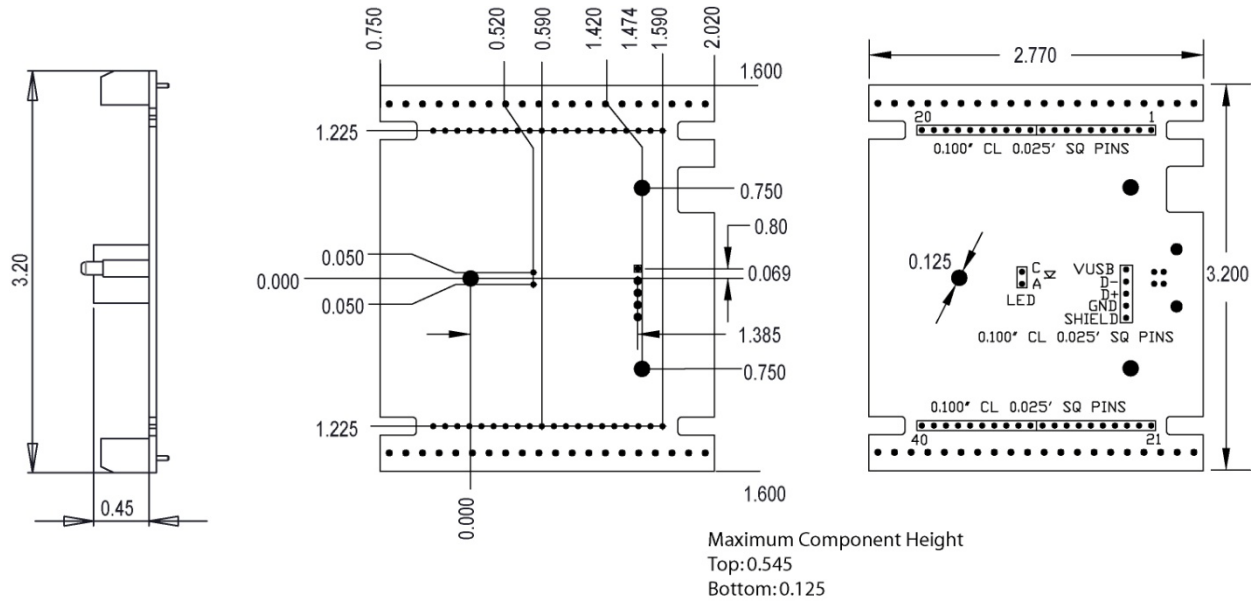
Mechanical drawings

Maximum Component Height
Top: 0.545
Bottom: 0.125

Figure 15. Circuit board (top) and enclosure dimensions

Specifications

All specifications are subject to change without notice.
Typical for 25°C unless otherwise specified.
Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

Parameter	Condition	Specification
A/D converter type		Successive approximation type
Input voltage range for linear operation	CHx to GND	Single-ended mode: ±10 V max
		Differential mode: –10 V min, +20 V max
Absolute maximum input voltage	*CHx to GND*	*±28 V max*
Input impedance		*122 kΩ*
Input current (Note 1)	Vin = +10 V	70 µA typ
	Vin = 0 V	–12 µA typ
	Vin = –10 V	–94 µA typ
Number of channels		8 single-ended or 4 differential; software-selectable
Input ranges	Single-ended	±10 V, G=2
	Differential	±20 V, G=1
		±10 V, G=2
		±5 V, G=4
		±4 V, G=5
		±2.5 V, G=8
		±2.0 V, G=10
		±1.25 V, G=16
		±1.0 V, G=20
		Software-selectable
Throughput (Note 2)	Software paced	250 S/s typ, PC-dependent
	Hardware paced	0.014 S/s to 48 kS/s
Channel gain queue		Software selectable. 8 elements in SE mode, 4 elements in DIFF mode.
		One gain element per channel. Elements must be unique and listed in ascending order.
Resolution (Note 3)	Differential	14 bits, no missing codes
	Single-ended	13 bits
Integral linearity error		±2 LSB typ
Differential linearity error		±0.5 LSB typ
Absolute accuracy long term drift (Note 4)	±20 V range	±3 LSB typ (Δt = 1000 hrs)
	±4 V range	±6 LSB typ (Δt = 1000 hrs)
	±1 V range	±8 LSB typ (Δt = 1000 hrs)
Trigger source		External digital: TRIG_IN
		Software-selectable

Note 1: Input current is a function of applied voltage on the analog input channels. For a given input voltage, Vin, the input leakage is approximately equal to $(8.181 * Vin – 12)$ µA.

Note 2: Maximum throughput when scanning is machine dependent.

Note 3: The ADS7871 converter only returns 13 bits (0 to 8,192 codes) in single-ended mode.

Note 4: Extrapolating the long term drift accuracy specifications will provide the approximate long term drift of the intermediate input ranges.

Accuracy

Table 2. Accuracy, differential mode

Range	Absolute Accuracy 25 °C (±mV)	Absolute Accuracy 0 °C to 50°C (±mV)
±20 V	10.98	49.08
±10 V	7.32	33.42
±5 V	3.66	20.76
±4 V	2.92	19.02
±2.5 V	1.83	14.97
±2 V	1.70	14.29
±1.25 V	1.21	12.18
±1 V	1.09	11.63

Table 3. Accuracy, single-ended mode

Range	Absolute Accuracy 25 °C (±mV)	Absolute Accuracy 0 °C to 50 °C (±mV)
±10 V	10.98	49.08

Noise performance

Table 4. Noise performance, differential mode

Range	Typical counts	Least significant bitroot $_{mean\ square}$ (LSBrms)
±20 V	8	1.21
±10 V	8	1.21
±5 V	9	1.36
±4 V	10	1.51
±2.5 V	12	1.81
±2 V	14	2.12
±1.25 V	18	2.72
±1 V	22	3.33

Table 5. Noise performance, single-ended mode

Range	Typical Counts	LSBrms
±10 V	8.0	1.21

Analog output

Table 6. Analog output specifications

Parameter	Condition	Specification
Resolution		12-bits, 1 in 4,096
Output range		*0 V to 5.0 V*
Number of channels		2
Throughput (Note 5)	Software paced	250 S/s single channel typ, PC dependent
	Hardware paced, per channel	50 kS/s max
Power on and reset voltage		0 V, ±20 mV typ; initializes to 000h code
Output drive	Each D/A OUT	5 mA, sourcing
Slew rate		0.8 V/ µs typ

Note 5: Maximum throughput when scanning is machine dependent.

Table 7. Analog output accuracy, all values are (±); accuracy tested at no load

Range	Accuracy (LSB)
0 V to 5.0 V	4.0 typ, 45.0 max

Table 8. Analog output accuracy components, all values are (±)

Range	% of FSR	Gain Error at FS (mV)	Offset (mV) (Note 6)	Accuracy at FS (mV)
0 V to 5.0 V	0.1 typ, 0.9 max	4.0 typ, 36.0 max	1.0 typ, 9.0 max	4.0 typ, 45.0 max

Note 6: Zero-scale offsets may result in a fixed zero-scale error producing a "dead-band" digital input code region. In this case, changes in digital input code at values less than 0x040 may not produce a corresponding change in the output voltage. The offset error is tested and specified at code 0x040.

Digital input/output

Table 9. Digital I/O specifications

Parameter	Specification
Digital type	CMOS
Number of I/O	16 (Port A0 through A7, Port B0 through B7)
Configuration	2 banks of 8. Port B is high current drive.
Pull up/pull-down configuration	All pins pulled up to 5V via 47 kΩ resistors (default). Change to pull-down using internal user-configurable jumpers.
Input high voltage threshold	2.0 V min
Input high voltage limit	5.5 V absolute max
Input low voltage threshold	0.8 V max
Input low voltage limit	–0.5 V absolute min 0 V recommended min
Output high voltage, Port A	4.4 V min (IOH = –20 µA) 3.84 V min (IOH = –6.0 mA)
Output low voltage, Port A	0.1 V max (IOL = 20 µA) 0.33 V max (IOL = 6.0 mA)
Output high voltage, Port B	4.4 V min (IOH = –50 µA) 3.76 V min (IOH = –24.0 mA)
Output low voltage, Port B	0.1 V max (IOH = 50 µA) 0.44 V max (IOH = 24.0 mA)
Power on and reset state	Input

External trigger

Table 10. Digital trigger specifications

Parameter	Specification
Trigger source (Note 7)	External digital; TRIG_IN terminal
Trigger mode	Edge sensitive; software-selectable for CMOS compatible rising or falling edge, high or low level.
Trigger latency	10 µs max
Trigger pulse width	1 µs min
Input type	Schmitt trigger, 47 kΩ pull-down to ground
Schmitt trigger hysteresis	1.01 V typ 0.6 V min 1.5 V max
Input high voltage threshold	2.43 V typ 1.9 V min 3.1V max
Input high voltage limit	5.5 V absolute max
Input low voltage threshold	1.42 V typ 1.0 V min 2.0 V max
Input low voltage limit	–0.5 V absolute min 0 V recommended min

External clock input/output

Table 11. External clock I/O specifications

Parameter	Condition	Specification
Terminal name		SYNC
Terminal type		Bidirectional
Direction (software-selectable)	Output	Outputs the internal A/D pacer clock. Active on rising edge.
	Input (default)	Receives A/D pacer clock from external source. Active on rising edge.
Input clock rate		48 kHz, max
Clock pulse width	Input mode	1 µs min
	Output mode	5 µs min
Input type		Schmitt trigger, 47 kΩ pull-down to ground
Schmitt trigger hysteresis		1.01 V typ 0.6 V min 1.5 V max
Input high voltage threshold		2.43 V typ 1.9 V min 3.1V max
Input high voltage limit		5.5 V absolute max
Input low voltage threshold		1.42 V typ 1.0 V min 2.0 V max
Input low voltage limit		–0.5 V absolute min 0 V recommended min
Output high voltage		4.4 V min (IOH = –50 µA) 3.80 V min (IOH = –8 mA)
Output low voltage		0.1 V max (IOL = 50 µA) 0.44 V max (IOL = 8 mA)

Counter

Table 12. Counter specifications

Parameter	Specification
Pin name	CTR
Counter type	Event counter
Number of channels	1
Input type	Schmitt trigger, 47 kΩ pull-down to ground, rising edge triggered
Input source	*CTR screw terminal*
Resolution	32 bits
Maximum input frequency	1 MHz
High pulse width	*500 ns min*
Low pulse width	*500 ns min*
Schmitt trigger hysteresis	1.01 V typ 0.6 V min 1.5 V max
Input high voltage threshold	2.43 V typ 1.9 V min 3.1V max
Input high voltage limit	5.5 V absolute max
Input low voltage threshold	1.42 V typ 1.0 V min 2.0 V max
Input low voltage limit	–0.5 V absolute min 0 V recommended min

Memory

Table 13. Memory specifications

Parameter	Specification
Non-volatile EEPROM	2,048 bytes (768 bytes calibration, 256 bytes user, 1,024 bytes DAQFlex)

Microcontroller

Table 14. Microcontroller specifications

Parameter	Specification
Type	*High performance 16-bit RISC microcontroller*

Power

Table 15. Power specifications

Parameter	Condition	Specification
Supply current	During USB enumeration	< 100 mA
	After USB enumeration, including DIO, AO, SYNC, and +VO output loading	< 500 mA
+VO power available	After USB enumeration	4.5 V min, 5.25 V max
+VO output current	After USB enumeration	100 mA max

General

Table 16. General specifications

Parameter	Specification
Device type	USB 2.0 full speed
Device compatibility	USB 1.1, USB 2.0

Environmental

Table 17. Environmental specifications

Parameter	Specification
Operating temperature range	0 °C to 70 °C
Storage temperature range	–40 °C to 70 °C
Humidity	0% to 90% non-condensing

Mechanical

Table 18. Mechanical specifications

Parameter	Specification
Dimensions (L × W × H)	79 × 82 × 27 mm (3.10 × 3.20 × 1.05 in.)
USB cable length	3 m (9.84 ft) max
User connection length	3 m (9.84 ft) max

Screw terminal connector

Table 19. Screw terminal specifications

Parameter	Specification
Connector type	Screw terminal
Wire gauge range	16 AWG to 30 AWG

Differential mode pinout

Table 20. 4-channel differential mode pinout

Pin	Signal name	Pin description	Pin	Signal name	Pin description
1	CH0 IN HI	Analog input 0+	21	Port A0	Port A bit 0
2	CH0 IN LO	Analog input 0–	22	Port A1	Port A bit 1
3	AGND	Analog ground	23	Port A2	Port A bit 2
4	CH1 IN HI	Analog input 1+	24	Port A3	Port A bit 3
5	CH1 IN LO	Analog input 1–	25	Port A4	Port A bit 4
6	AGND	Analog ground	26	Port A5	Port A bit 5
7	CH2 IN HI	Analog input 2+	27	Port A6	Port A bit 6
8	CH2 IN LO	Analog input 2–	28	Port A7	Port A bit 7
9	AGND	Analog ground	29	GND	Ground
10	CH3 IN HI	Analog input 3+	30	+VO	Power output
11	CH3 IN LO	Analog input 3–	31	GND	Ground
12	AGND	Analog ground	32	Port B0	Port B bit 0
13	D/A OUT 0	Analog output 0	33	Port B1	Port B bit 1
14	D/A OUT 1	Analog output 1	34	Port B2	Port B bit 2
15	AGND	Analog ground	35	Port B3	Port B bit 3
16	Reserved	Reserved for future use	36	Port B4	Port B bit 4
17	GND	Ground	37	Port B5	Port B bit 5
18	TRIG_IN	Trigger input	38	Port B6	Port B bit 6
19	SYNC	Synchronization I/O	39	Port B7	Port B bit 7
20	CTR	Counter input	40	GND	Ground

Single-ended mode pinout

Table 21. 8-channel single-ended mode pinout

Pin	Signal name	Pin description	Pin	Signal name	Pin description
1	CH0 IN	Analog input 0	21	Port A0	Port A bit 0
2	CH1 IN	Analog input 1	22	Port A1	Port A bit 1
3	AGND	Analog ground	23	Port A2	Port A bit 2
4	CH2 IN	Analog input 2	24	Port A3	Port A bit 3
5	CH3 IN	Analog input 3	25	Port A4	Port A bit 4
6	AGND	Analog ground	26	Port A5	Port A bit 5
7	CH4 IN	Analog input 4	27	Port A6	Port A bit 6
8	CH5 IN	Analog input 5	28	Port A7	Port A bit 7
9	AGND	Analog ground	29	GND	Ground
10	CH6 IN	Analog input 6	30	+VO	Power output
11	CH7 IN	Analog input 7	31	GND	Ground
12	AGND	Analog ground	32	Port B0	Port B bit 0
13	D/A OUT 0	Analog output 0	33	Port B1	Port B bit 1
14	D/A OUT 1	Analog output 1	34	Port B2	Port B bit 2
15	AGND	Analog ground	35	Port B3	Port B bit 3
16	Reserved	Reserved for future use	36	Port B4	Port B bit 4
17	GND	Ground	37	Port B5	Port B bit 5
18	TRIG_IN	Trigger input	38	Port B6	Port B bit 6
19	SYNC	Synchronization I/O	39	Port B7	Port B bit 7
20	CTR	Counter input	40	GND	Ground