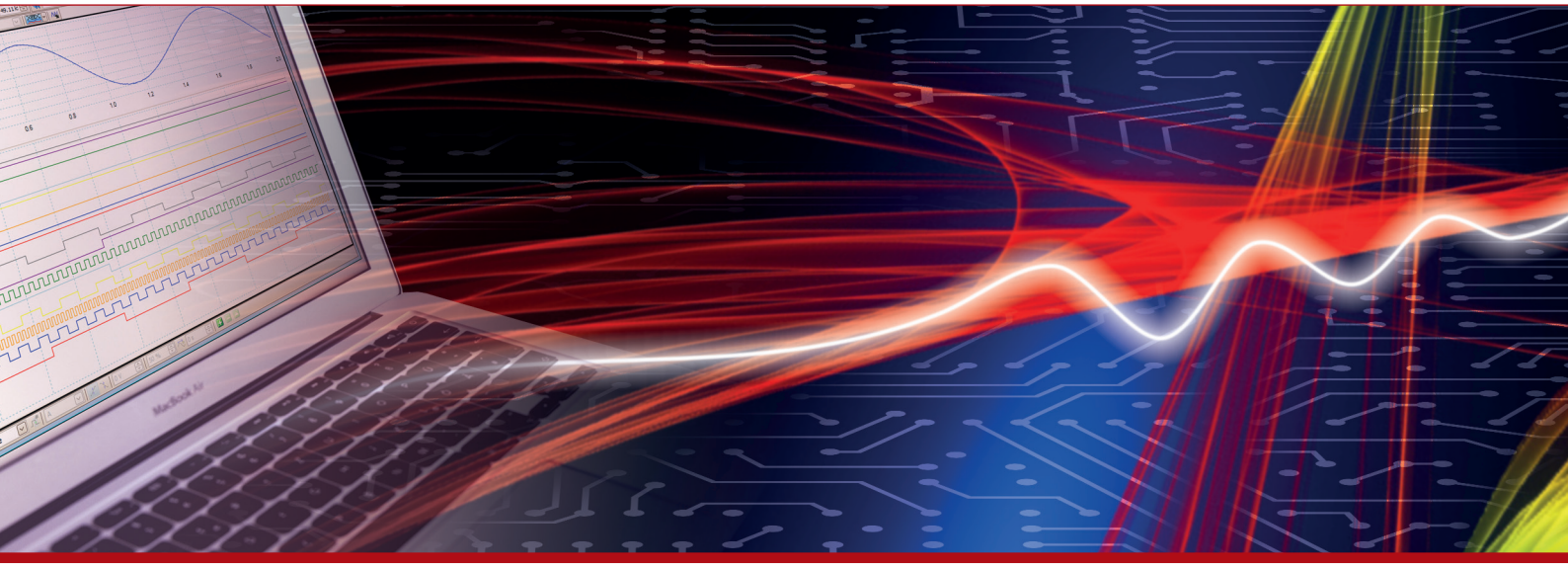
Product Datasheet - Technical Specifications



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Mechanical drawings

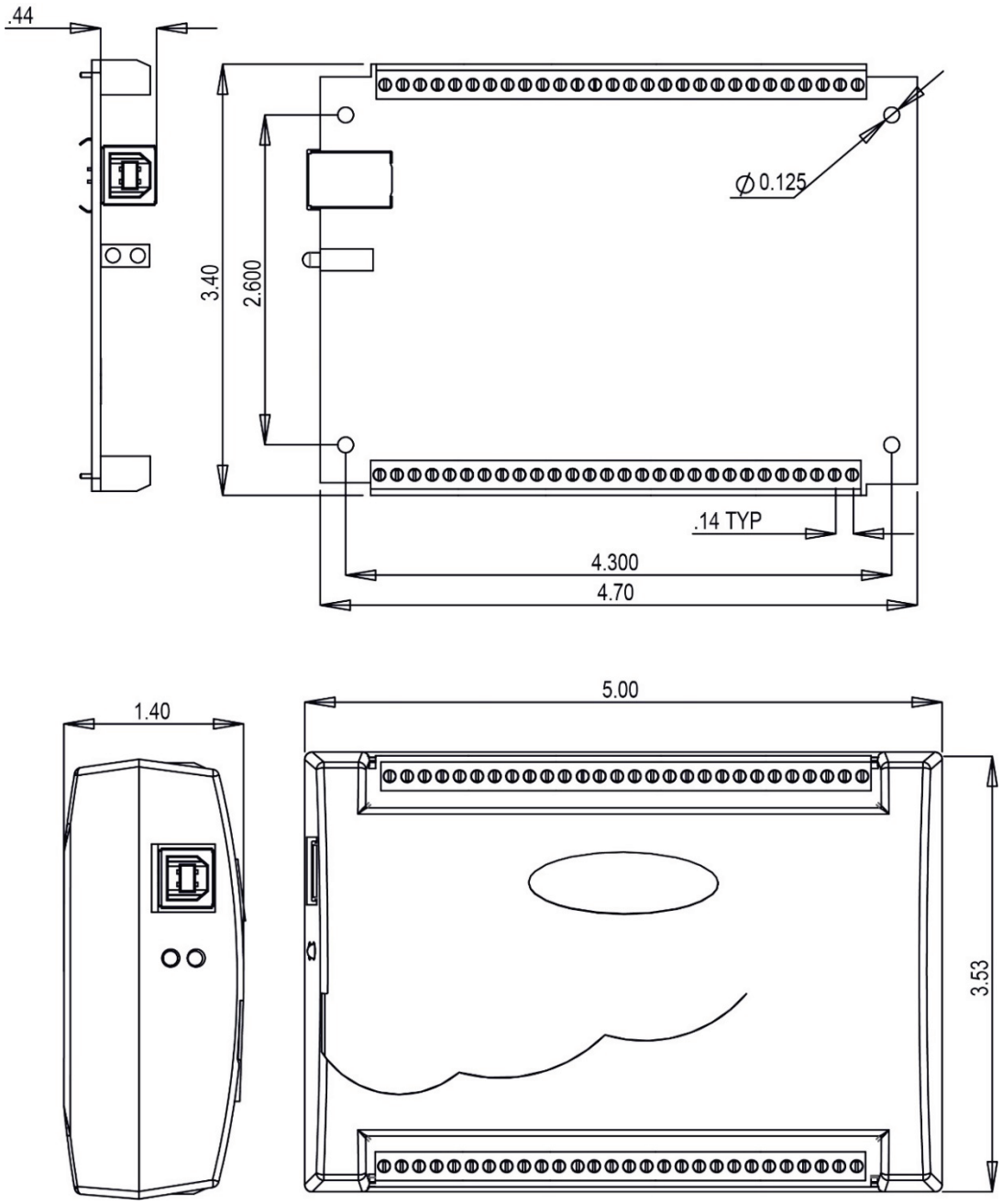

Figure 11. RedLab 1808 circuit board (top) and enclosure dimensions

Specifications

All specifications are subject to change without notice.
Typical for 25 °C unless otherwise specified.
Specifications in *italic* text are guaranteed by design.

Analog input

Table 1. General analog input specifications

Parameter	Condition	Specification
A/D converter type		Simultaneous
ADC resolution		18 bits
Number of channels		8 differential (DIFF), 8 single-ended (SE); software-selectable per-channel for SE or DIFF
Input voltage range		±10 V, ±5 V, 0 V to 10 V, 0 V to 5 V Software-selectable per channel
Absolute max input voltage	*CHx relative to AGND*	■ *±25 V max (power on)* ■ *±15 V max (power off)*
Input impedance		■ *>1 GΩ (power on)* ■ *1000 Ω (power off)*
Input bias current		*±50 pA*
Input bandwidth	All input ranges, small signal (–3 dB)	2.0 MHz
Input capacitance		*50 pf*
Common mode voltage range	±10 V range	±10.1 V
	±5 V range	±10.1 V
	0 V to 10 V range	±10.1 V
	0 V to 5 V range	±10.1 V
Common mode rejection ratio	*fIN* ≤ 1 kHz, all input ranges	90 dB
Crosstalk	±10 V, adjacent channels, DC to 100 kHz	–95 dB
Input coupling		DC
Sample rate		0.023 Hz to 50 kHz; software-selectable
Scan clock source		Internal input scan clock or external input scan clock (ICLKI pin)
Trigger source		■ ITRIG (see *External trigger on page 21*) ■ Digital pattern detection (see *Pattern trigger* on page 21)
Channel gain queue	Up to 8 elements	Software-selectable. Queue list may contain up to eight elements of unique, consecutive channels paired with any valid range.
Warm-up time		15 minutes min

Accuracy

Analog input DC voltage measurement accuracy

Table 2. DC accuracy components and specifications. All values are (±)

Range	Gain error (% of reading)	Offset error (mV)	INL error (% of range)	Absolute accuracy at Full Scale (mV)	Gain temperature coefficient (% reading/°C)	Offset temperature coefficient (µV/°C)
±10 V	0.020	1.5	0.00076	3.576	0.00023	4
±5 V	0.020	1.0	0.00057	2.028	0.00023	4
0 V to 10 V	0.020	1.5	0.00028	3.528	0.00023	4
0 V to 5 V	0.020	1.0	0.00014	2.007	0.00023	4

Dynamic performance

Table 3. Dynamic performance specifications

Range	Condition	Specification
±10 V	*Signal-to-noise ratio (SNR)*	*94 dB*
	Signal-to-noise-and-distortion ratio (SINAD)	*94 dB*
	Total harmonic distortion (THD)	*–108 dB*
	Spurious free dynamic range (SFDR)	*112 dB*
	Effective number of bits (ENOB)	*15.3 bits*
±5 V	*SNR*	*91 dB*
	SINAD	*91 dB*
	THD	*–105 dB*
	SFDR	*107 dB*
	ENOB	*14.8 bits*
0 V to 10 V	*SNR*	*87 dB*
	SINAD	*87 dB*
	THD	*–104 dB*
	SFDR	*109 dB*
	ENOB	*14.5 bits*
0 V to 5 V	*SNR*	*83 dB*
	SINAD	*83 dB*
	THD	*–103 dB*
	SFDR	*103 dB*
	ENOB	*13.6 bits*

Noise performance

For the peak-to-peak noise distribution test, a differential input channel is connected to AGND at the input terminal block, and 32,000 samples are acquired at the maximum rate available at each setting.

Table 4. Noise performance specifications

Range	Counts	LSBrms
±10 V	11.6	1.77
±5 V	18.0	2.73
0 V to 10 V	23.3	3.54
0 V to 5 V	36.1	5.47

Analog output

Table 5. Analog output specifications

Parameter	Condition	Specification
Number of channels		2
Resolution		16 bits
Output ranges	Calibrated	±10 V
Output transient	Host computer is reset, powered on, suspended, or a reset command is issued to the device	Duration: 5 ms Amplitude: 2 V p-p
	Powered off from 0 V output	Duration: 20 ms Amplitude: 5 V p-p
Differential non-linearity		±0.25 LSB typ ±1 LSB max
Output current	AOUTx pins	±3.5 mA max
Output short-circuit protection	Single AOUTx channel connected to AGND	Unlimited duration
Output coupling		DC
Power on and reset state		DACs cleared to zero-scale: 0 V, ±50 mV
Output noise		100 µVrms
Trigger source		■ OTRIG (see *External trigger* on page 21) ■ Digital pattern detection (see *Pattern trigger* on page 21)
Scan clock source		Internal output scan clock or external output scan clock (OCLKI pin)
Output update rate		0.023 Hz to 125 kHz per channel
Slew rate		*15 V/µS*
Throughput	Software paced	33 S/s to 8,000 S/s typ, system-dependent
	Hardware paced	250 kS/s max, system-dependent

Note 1: Leave unused AOUTx output channels disconnected.

Note 2: AOUTx defaults to 0 V whenever the host computer is reset, powered on, suspended, or a reset command is issued to the device.

Table 6. Calibrated absolute accuracy specifications

Range	Absolute accuracy (±LSB)
±10 V	16

Table 7. Calibrated absolute accuracy components specifications

Range	% of reading	Offset (±mV)	Offset tempco (µV/°C)	Gain tempco (ppm of range/°C)
±10 V	0.0183	1.831	4.7	9.4

Table 8. Relative accuracy specifications (±LSB)

Range	Relative accuracy (INL)
±10 V	1.0

Analog input/output calibration

Table 9. Analog I/O calibration specifications

Parameter	Specification
Warm-up time	15 minutes recommended min
Calibration method	Factory calibration
Calibration interval	1 year

Digital input/output

Table 10. Digital I/O specifications

Parameter	Specification
Digital type	CMOS
Number of I/O	4
Configuration	Each bit may be configured as input (power on default) or output
Pull-up configuration	The port has 47 kΩ resistors configurable as pull-up or pull-down (default) via internal jumper (DIO).
Digital I/O transfer rate (system-paced, asynchronous)	33 to 8,000 port reads/writes or single bit reads/writes per second typ, system dependent.
Digital I/O transfer rate (synchronous)	0.023 Hz to 50 kHz input, 125 kHz output, based on the internal clock speed of 100 MHz
Scan clock source for input	Internal input scan clock or external input scan clock (ICLKI pin)
Scan clock source for input	Internal output scan clock or external output scan clock (OCLKI pin)
Trigger source	■ ITRIG for inputs, OTRIG for outputs (see *External trigger* on page 21) ■ Digital pattern detection for inputs and outputs (see *Pattern trigger* on page 21)
Input high voltage	2.0 V min 5.5 V absolute max
Input low voltage	0.8 V max –0.5 V absolute min 0 V recommended min
Output high voltage	4.4 V min (IOH = –50 µA) 3.76 V min (IOH = –2.5 mA)
Output low voltage	0.1 V max (IOL = 50 µA) 0.44 V max (IOL = 2.5 mA)
Output current	±2.5 mA max

Counter

Table 11. Counter specifications

Parameter	Specification
Terminal names	CTR0, CTR1
Number of channels	2 channels
Resolution	32-bit
Counter type	FPGA
Counter input modes	Totalize, Pulse width, Period
Input type	Schmitt trigger, 33 Ω series resistor, 47 kΩ pull-down to ground
Input source	CTR0 CTR1
Scan clock source	Internal input scan clock or external input scan clock (ICLKI pin)
Trigger source	■ ITRIG (see *External trigger* on page 21) ■ Digital pattern detection (see *Pattern trigger* on page 21)
Counter read clock	Internal or external input scan clock up to 50 kHz
Period/pulse width resolution	20 ns, 200 ns, 2 µs or 20 µs; software-selectable
Input high voltage	2.2 V min, 5.5 V max
Input low voltage	1.5 V max, –0.5 V min
Schmitt trigger hysteresis	0.4 V min, 1.2 V max
Input frequency	50 MHz, max
Schmitt trigger hysteresis	0.76 V typ 0.4 V min 1.2 V max
Input high voltage threshold	1.74 V typ 1.3 V min 2.2 V max
Input low voltage threshold	0.98 V typ 0.6 V min 1.5 V max
Input low voltage limit	–0.5 V absolute min 0 V recommended min

Quadrature inputs

Table 12. Quadrature input specifications

Parameter	Specification
Terminal names	ENC0A, ENC0B, ENC0Z; ENC1A, ENC1B, ENC1Z
Number of encoders	2
Signals per encoder	A, B and Z
Resolution	20 ns
Maximum frequency	50 MHz
Minimum pulse width	*10 ns*
De-bounce function	None
Scan clock source	Internal input scan clock or external input scan clock (ICLKI pin)
Trigger source	■ ITRIG (see *External trigger* on page 21) ■ Digital pattern detection (see *Pattern trigger* on page 21)
Input high voltage	2.2 V min, 5.5 V max
Input low voltage	1.5 V max, –0.5 V min
Absolute maximum input voltage	5.5 V

Timer

Table 13. Timer specifications

Parameter	Specification
Terminal name	TMR0, TMR1
Timer type	PWM output with count, period, delay, and pulse width registers
Output value	Default state is idle low with pulses high, software-selectable output invert
Trigger source	OTRIG (see *External trigger* on page 21)
Internal clock frequency	100 MHz
Register widths	32-bit
High pulse width	*10 ns min*
Low pulse width	*10 ns min*
Output high voltage	4.4 V min (IOH = –50 µA) 3.76 V min (IOH = –2.5 mA)
Output low voltage	0.1 V max (IOL = 50 µA) 0.44 V max (IOL = 2.5 mA)
Output current	±2.5 mA max

External clock input/output

Table 14. External clock I/O specifications

Parameter	Specification	
Terminal names	ICLKI, ICLKO OCLKI, OCLKO	
Terminal types	xCLKI: xCLKO:	Input, active on rising edge Output, power on default is 0 V, active on rising edge
Terminal descriptions	xCLKI:	Receives sampling clock from external source
	xCLKO:	Outputs the internal input scan or internal output scan clock, or the pulse generated from xCLKI when in external clock mode.
Input clock rate	125 kHz max	
Clock pulse width	xCLKI:	400 ns min
	xCLKO:	400 ns min
Input type	Schmitt trigger, 33 Ω series resistor, 47 kΩ pull-down to ground	
Schmitt trigger hysteresis	0.4 V to 1.2 V	
Input high voltage	2.2 V min 5.5 V absolute max	
Input low voltage	1.5 V max –0.5 V absolute min 0 V recommended min	
Output high voltage	4.4 V min (IOH = –50 µA) 3.76 V min (IOH = –2.5 mA)	
Output low voltage	0.1 V max (IOL = 50 µA) 0.44 V max (IOL = 2.5 mA)	
Output current	±2.5 mA max	

External trigger

Table 15. External trigger specifications

Parameter	Specification
Trigger source	ITRIG for inputs, OTRIG for outputs
Trigger mode	Software programmable for edge or level sensitive, rising or falling edge, high or low level. Power on default is edge sensitive, rising edge.
Trigger latency	1 µs + 1 clock cycle max
Trigger pulse width	100 ns min
Input type	Schmitt trigger, 33 Ω series resistor and 49.9 kΩ pull-down to ground
Schmitt trigger hysteresis	0.4 V to 1.2 V
Input high voltage	2.2 V min 5.5 V absolute max
Input low voltage	1.5 V max –0.5 V absolute min 0 V recommended min

Pattern trigger

Table 16. Pattern trigger specifications

Parameter	Specification
Trigger source	DIO0 – DIO3
Trigger types	Above pattern, Below pattern, Equal pattern, or Not equal pattern
Trigger stability	Digital port must be stable for 50 ns to be recognized as a pattern
Trigger bit width	Up to 4, adjustable through bitmask
Trigger latency	Up to 1 scan period

Memory

Table 17. Memory specifications

Parameter	Specification
Data FIFO	4 kS analog input/2 kS analog output
Non-volatile memory	32 KB (28 KB firmware storage, 4 KB calibration/user data)

Power

Table 18. Power specifications

Parameter	Condition	Specification
Supply current (Note 3)	Quiescent current	305 mA
+VO user output voltage range (Note 4)	Available at connector pin 13	4.5 V min to 5.25 V max
+VO user output current	Available at connector pin 13	10 mA max

Note 3: This is the total quiescent current requirement for the device that includes up to 10 mA for the status LED. This does not include any potential loading of the digital I/O bits, +VO terminal, or the AOUTx outputs.

Note 4: The +4.5 V min limit includes the +VO 10 mA load, it does not include any potential loading of the digital I/O bits or the AOUTx outputs.

USB

Table 19. USB specifications

Parameter	Specification
USB device type	USB 2.0 (high-speed)
Device compatibility	USB 1.1, USB 2.0, USB 3.0
USB cable type	A-B cable, UL type AWM 2725 or equivalent. (Min 24 AWG VBUS/GND, min 28 AWG D+/D–)
USB cable length	3 m (9.84 ft) max

Environmental

Table 20. Environmental specifications

Parameter	Specification
Operating temperature range	0 °C to 55 °C max
Storage temperature range	–40 °C to 85 °C max
Humidity	0% to 90% non-condensing max

Mechanical

Table 21. Mechanical specifications

Parameter	Specification
Dimensions (L × W × H)	127 × 89.9 × 35.6 mm (5.00 × 3.53 × 1.40 in.)
User connection length	3 m (9.84 ft) max

Screw terminal connector

Table 22. Screw terminal connector specifications

Parameter	Specification
Connector type	Screw terminal
Wire gauge range	16 AWG to 30 AWG

Differential mode pinout

Table 23. 8-channel differential mode pinout

Terminal			Terminal		
#	**Label**	**Use**	**#**	**Label**	**Use**
1	CH0H	AI channel 0 HI	29	CH7L	AI channel 7 LO
2	CH0L	AI channel 0 LO	30	CH7H	AI channel 7 HI
3	AGND	Analog ground	31	AGND	Analog ground
4	CH1H	AI channel 1 HI	32	CH6L	AI channel 6 LO
5	CH1L	AI channel 1 LO	33	CH6H	AI channel 6 HI
6	AGND	Analog ground	34	AGND	Analog ground
7	CH2H	AI channel 2 HI	35	CH5L	AI channel 5 LO
8	CH2L	AI channel 2 LO	36	CH5H	AI channel 5 HI
9	AGND	Analog ground	37	AGND	Analog ground
10	CH3H	AI channel 3 HI	38	CH4L	AI channel 4 LO
11	CH3L	AI channel 3 LO	39	CH4H	AI channel 4 HI
12	AGND	Analog ground	40	AGND	Analog ground
13	+VO	+5V power output	41	AOUT0	AO channel 0
14	AGND	Analog ground	42	AOUT1	AO channel 1
15	GND	Digital Ground	43	AGND	Analog ground
16	TMR0	Timer 0 output	44	GND	Digital Ground
17	TMR1	Timer 1 output	45	DIO0	DIO channel 0
18	ICLKO	Input scan clock output	46	DIO1	DIO channel 1
19	OCLKO	Output scan clock output	47	GND	Digital Ground
20	GND	Digital ground	48	DIO2	DIO channel 2
21	ICLKI	Input scan clock input	49	DIO3	DIO channel 3
22	OCLKI	Output scan clock input	50	GND	Digital Ground
23	ITRIG	Input Trigger	51	CTR0	Counter 0 input
24	OTRIG	Output Trigger	52	CTR1	Counter 1 input
25	GND	Digital ground	53	GND	Digital ground
26	ENC1A	Encoder 1 Input A	54	ENC0A	Encoder 0 Input A
27	ENC1B	Encoder 1 Input B	55	ENC0B	Encoder 0 Input B
28	ENC1Z	Encoder 1 Input Z	56	ENC0Z	Encoder 0 Input Z

Single-ended mode pinout

Table 24. 16-channel single-ended mode pinout

Terminal			Terminal		
#	**Label**	**Use**	**#**	**Label**	**Use**
1	CH0H	AI channel 0 HI	29	NC	No connection
2	NC	No connection	30	CH7H	AI channel 7 HI
3	AGND	Analog ground	31	AGND	Analog ground
4	CH1H	AI channel 1 HI	32	NC	No connection
5	NC	No connection	33	CH6H	AI channel 6 HI
6	AGND	Analog ground	34	AGND	Analog ground
7	CH2H	AI channel 2 HI	35	NC	No connection
8	NC	No connection	36	CH5H	AI channel 5 HI
9	AGND	Analog ground	37	AGND	Analog ground
10	CH3H	AI channel 3 HI	38	NC	No connection
11	NC	No connection	39	CH4H	AI channel 4 HI
12	AGND	Analog ground	40	AGND	Analog ground
13	+VO	+5V power output	41	AOUT0	AO channel 0
14	AGND	Analog ground	42	AOUT1	AO channel 1
15	GND	Digital Ground	43	AGND	Analog ground
16	TMR0	Timer 0 output	44	GND	Digital Ground
17	TMR1	Timer 1 output	45	DIO0	DIO channel 0
18	ICLKO	Input scan clock output	46	DIO1	DIO channel 1
19	OCLKO	Output scan clock output	47	GND	Digital Ground
20	GND	Digital ground	48	DIO2	DIO channel 2
21	ICLKI	Input scan clock input	49	DIO3	DIO channel 3
22	OCLKI	Output scan clock input	50	GND	Digital Ground
23	ITRIG	Input Trigger	51	CTR0	Counter 0 input
24	OTRIG	Output Trigger	52	CTR1	Counter 1 input
25	GND	Digital ground	53	GND	Digital ground
26	ENC1A	Encoder 1 Input A	54	ENC0A	Encoder 0 Input A
27	ENC1B	Encoder 1 Input B	55	ENC0B	Encoder 0 Input B
28	ENC1Z	Encoder 1 Input Z	56	ENC0Z	Encoder 0 Input Z